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GaNSafe™

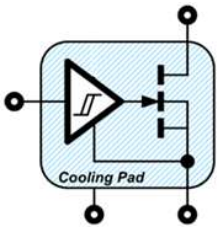
NV6515

PRELIMINARY DATASHEET

GaNSafe™ Power IC

CERTIFIED CARBON NEUTRAL company
CarbonNeutral.com

Bottom-cooled TOLL-4L



Simplified Diagram

1. Features

- V_{DS} 650V continuous / 800V transient
- 35 mΩ $R_{DS(ON)\_MAX\_25C}$ and 58 A $I_{DS(CONTINUOUS)}$
- TOLL-4L thermally-enhanced, bottom-cooled
- PWM input compatibility 10 to 20 V
- Paralleling capability up to 2x power ICs
- Zero reverse-recovery charge
- Turn-ON and Turn-OFF dV/dt programmability
- Up to 2 MHz operation
- Short Circuit Protection with 350 ns latency
- dV/dt immunity up to 100 V/ns
- 2kV ESD all Pins
- AEC-Q100 Grade 1 (ordering option)
- RoHS, Pb-free, REACH-compliant

2. Applications / Topologies

- AC-DC, DC-DC, DC-AC, and ZVS, CCM
- Half-bridge, full-bridge, 3-phase, buck/boost
- Data Center CRPS, and PV Inverter/ESS
- EV OBC & DC-DC converter, and motor drive

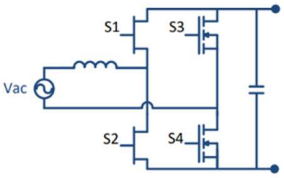
3. Description

The NV6515 is a thermally-enhanced bottom-cooled SMD version of the GaNFast™ power IC family, optimized for higher power systems using GaNSafe™ technology, making it the ideal choice for high-frequency, high-power-density, and high-efficiency power systems in data center, solar, industrial, and automotive segments.

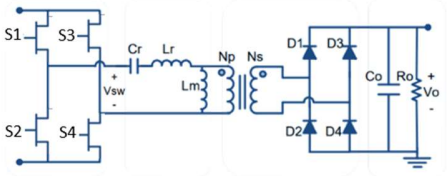
GaNFast power ICs integrate GaN FET(s) with gate drive to create an easy-to-use power stage building block.

GaNSafe technology further integrates critical protection and performance features that enable unprecedented reliability and robustness. The TOLL package ties this architecture together with industry-standard thermally-enhanced packaging, creating dependable solutions for world-class size/weight, efficiency, and cost.

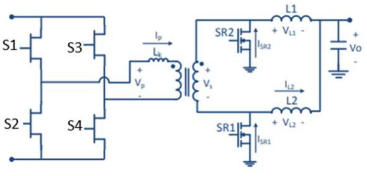
4. Typical Application Circuits



BTP PFC



CLLC or LLC



PSFB or DAB

5. Table of Contents

6. Absolute Maximum Ratings (Note 1) (with respect to Source, T_{CASE} = 25°C, unless specified)

Symbol	Parameter	Max	Units
$V_{DS(CONT)}$	Continuous Drain-to-Source voltage	-7 to +650	V
$V_{DS(TRAN)}$	Transient Drain-to-Source voltage (Note 2)	800	V
$I_{DS(CONT)}$	Continuous Drain current (T_{CASE} = 25 °C) (Note 3) Continuous Drain current (T_{CASE} = 100 °C, T_{JUNC} = 150 °C) (Note 3)	58 43	A
I_{DS_PULSE}	Pulsed Drain current (10 µs @ T_{JUNC} = 25 °C) (Note 3) Pulsed Drain current (10 µs @ T_{JUNC} = 150 °C) (Note 3)	119 43	A
V_{DRIVE_CONT}	Continuous input voltage measured between V_{DRIVE} and SK pins	-0.6 to 20	V
V_{DRIVE_TRANS}	Transient input voltage measured between V_{DRIVE} and SK pins (Note 4)	-2.0	V
dV/dt	Slew Rate on Drain-to-Source	100	V/ns
T_{JUNC}	Junction Temperature	-40 to +150	°C
T_{STOR}	Storage temperature	-55 to +150	°C

(1) Absolute Maximum Ratings are stress ratings, and subjecting devices to stresses beyond these ratings may cause permanent damage.

(2) $V_{DS\ (TRAN)}$ allows for surge ratings during ***non-repetitive*** events that are < 100 µs.

(3) Limited by Short Circuit Protection.

(4) Limited to 200 ns.

7. Recommended Operating Conditions (Note 5)

Symbol	Parameter	Min	Typ	Max	Units
V_{DRIVE_H}	Drive input pin voltage high	11	15	18	V
V_{DRIVE_L}	Drive input pin voltage low	-0.3	0	0.3	V
R_{DRIVE_ON}	Turn-ON V_{DRIVE} Pin series resistor	2.2		50	Ω
R_{DRIVE_OFF}	Turn-OFF V_{DRIVE} Pin series resistor	2.2		25	Ω

(5) Exposure to conditions beyond maximum recommended operating conditions for extended periods of time may affect device reliability.

8. ESD Ratings

Symbol	Parameter	Max	Units
HBM	Human Body Model (per JS-001-2014)	2,000	V
CDM	Charged Device Model (per JS-002-2014)	1,000	V

9. Thermal Resistance

Symbol	Parameter	Max	Units
$R_{e\_JUNC-CASE}$	Junction-to-Case Thermal Resistance	0.38	°C/W

10. Electrical Characteristics

Conditions unless otherwise specified: V_{DS} = 400V, V_{DRIVE} = 15V, T_{CASE} = 25°C, I_{DS} = 22A, R_{DRIVE} = 2.2Ω

Symbol	Parameter	Min	Typ	Max	Units	Conditions
Drive Pin Characteristics						
$I_{DRIVE\_OPERATING}$	V_{DRIVE} operating current		3.6		mA	V_{DRIVE} = 15V, F_{SW} = 300kHz, 50% D.C., V_{DS} = 0V
$I_{DRIVE\_LEAKAGE}$	V_{DRIVE} leakage current		1.5		mA	V_{DRIVE} = 15V
Switching Characteristics						
t_{ON}	Turn-ON propagation delay	25		36	ns	Fig 1,2 ; -40 ^{0}C ≤ T_{CASE} ≤ +125 ^{0}C ; R_{DRIVE} = 1Ω
t_{OFF}	Turn-OFF propagation delay	8		17	ns	Fig 1,2 ; -40 ^{0}C ≤ T_{CASE} ≤ +125 ^{0}C ; R_{DRIVE} = 1Ω
t_{ON_MIN}	Minimum Drive on-time pulse duration	75			ns	R_{DRIVE} = 1Ω
Short Circuit Protection (SCP)						
V_{DS_SCP}	$V_{DS(ON)}$ Short Circuit Detect Threshold	11.5	13.5		V	18V ≥ V_{DRIVE} ≥ 11V, T_{JUNC} = -40 °C to +150 °C, verified by design
$t_{SCP\_DLY\_TURN-ON}$	Delay from Short Circuit Event to Soft Shut Down, into Turn-ON		350		ns	18V ≥ V_{DRIVE} ≥ 11V, T_{JUNC} = -40 °C to +150 °C, verified by design
$t_{SCP\_DLY\_OPER}$	Delay from Short Circuit Event to Soft Shut Down, during Operation		50		ns	18V ≥ V_{DRIVE} ≥ 11V, T_{JUNC} = -40 °C to +150 °C, verified by design
GaN FET Characteristics						
I_{DSS}	Drain-Source leakage current		1.2		µA	V_{DS} = 650 V, V_{DRIVE} = 0 V
I_{DSS}	Drain-Source leakage current		118		µA	V_{DS} = 650 V, V_{DRIVE} = 0 V, T_{JUNC} = 150 °C
$R_{DS(ON)}$	Drain-Source resistance		25	35	mΩ	V_{DRIVE} = 15V
$R_{DS(ON)}$	Drain-Source resistance		60		mΩ	V_{DRIVE} = 15V, T_{JUNC} = 150 °C
V_{SD}	Source-Drain reverse voltage		3.3		V	V_{DRIVE} = 0 V, I_{SD} = 22 A
I_{SD}	Source-Drain reverse current		110		A	V_{DRIVE} = 0V, V_{DS} = 7V, 50us pulse, based on $P_{DISSIPATION}$
Q_{OSS}	Output charge		92		nC	V_{DS} = 400 V, V_{DRIVE} = 0 V
Q_{RR}	Reverse recovery charge		Zero		nC	
C_{OSS}	Output capacitance		108		pF	V_{DS} = 400 V, V_{DRIVE} = 0 V
$C_{O(er)}$ (Note 4)	Effective output capacitance, energy related		152		pF	V_{DS} = 400 V, V_{DRIVE} = 0 V
$C_{O(tr)}$ (Note 5)	Effective output capacitance, time related		229		pF	V_{DS} = 400 V, V_{DRIVE} = 0 V
E_{ON}	Switching energy, Turn-ON		80		µJ	V_{DS} = 400 V, R_{DRIVE} = 1Ω
E_{OFF}	Switching energy, Turn-OFF		12		µJ	V_{DS} = 0 to 400 V

(6) $C_{O(er)}$ is a fixed capacitance that gives the same stored energy as C_{OSS} while V_{DS} is rising from 0 to 400 V

(7) $C_{O(tr)}$ is a fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 400 V

11. Inductive Switching Test Circuit and Typical Waveforms

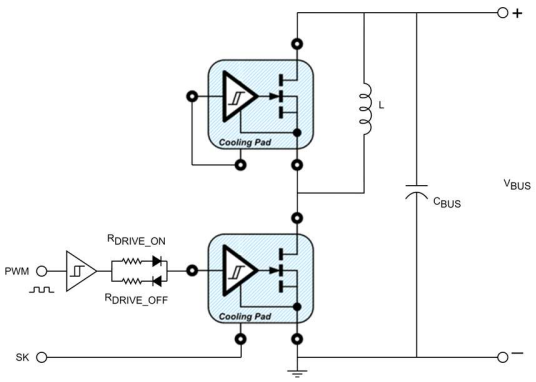


Figure 1. Inductive Switching Test Circuit

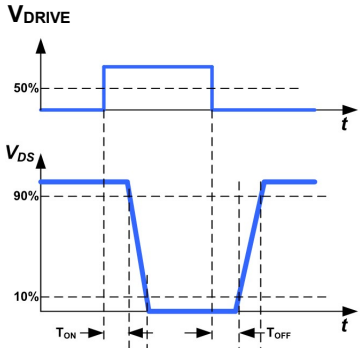


Figure 2. Prop Delay, Rise/Fall Time

12. Electrical Curves (GaN FET, T_{CASE} = 25 °C unless otherwise specified)

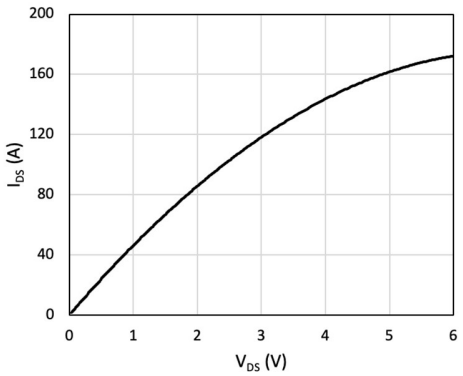


Fig. 3. I_{DS} vs. V_{DS}, T_{JUNC} = 25 °C

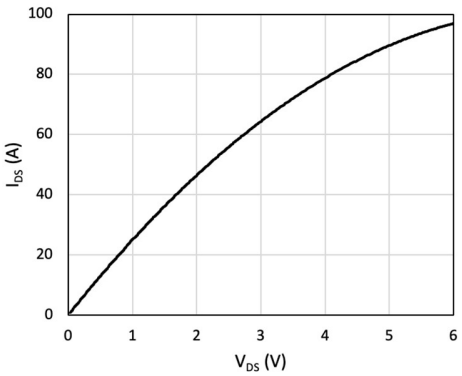


Fig. 4. I_{DS} vs. V_{DS}, T_{JUNC} = 150 °C

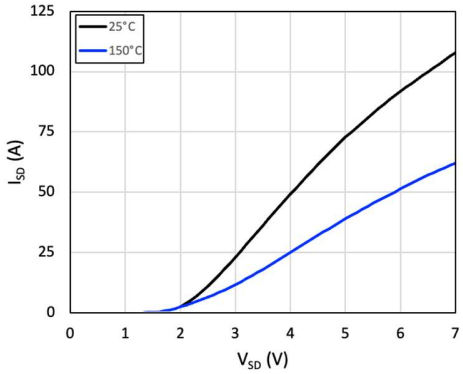


Fig. 5. I_{SD} vs. V_{SD}, T_{JUNC} = 25 °C, 150 °C

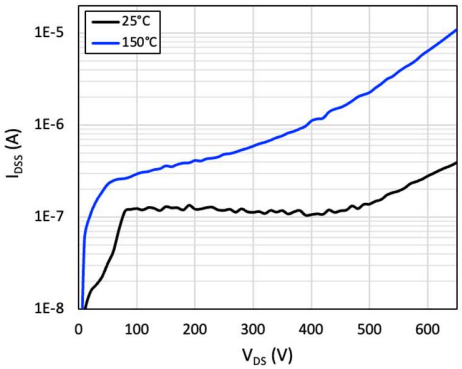


Fig. 6. I_{DSS} vs. V_{DS}, T_{JUNC} = 25 °C, 150 °C

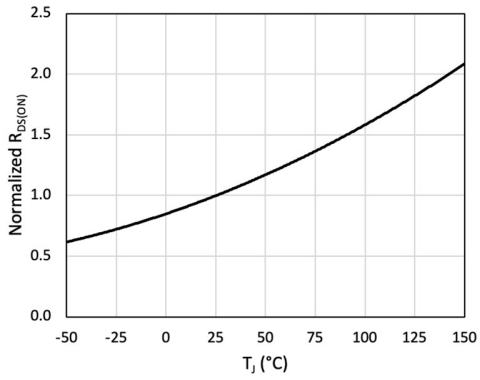


Fig. 7. Normalized R_{DSON} vs. T_{JUNC}

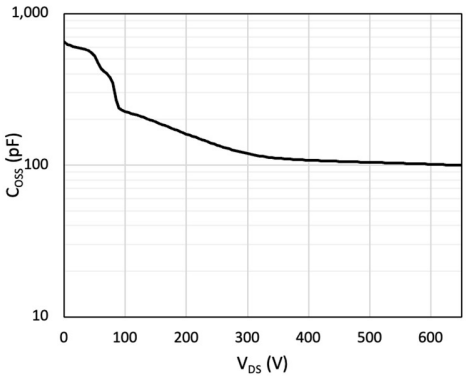


Fig. 8. C_{OSS} vs. V_{DS}

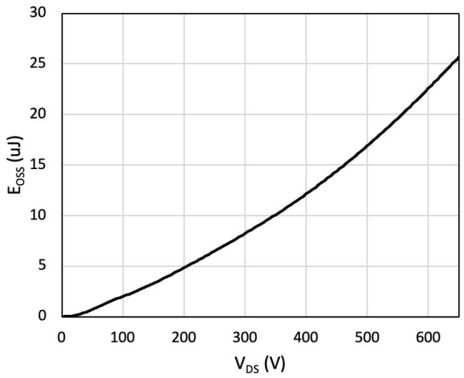


Fig. 9. E_{OSS} vs. V_{DS}

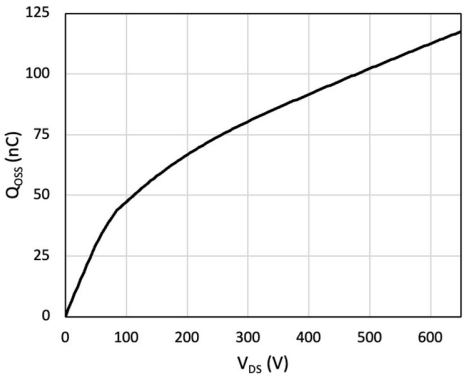


Fig. 10. Q_{OSS} vs. V_{DS}

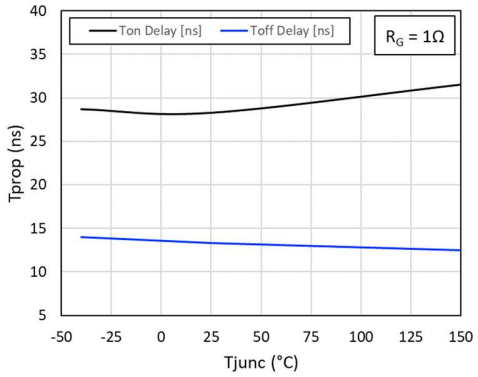


Fig. 11. $t_{PROP\_ON\ ,\ OFF}$ vs. T_{JUNC}

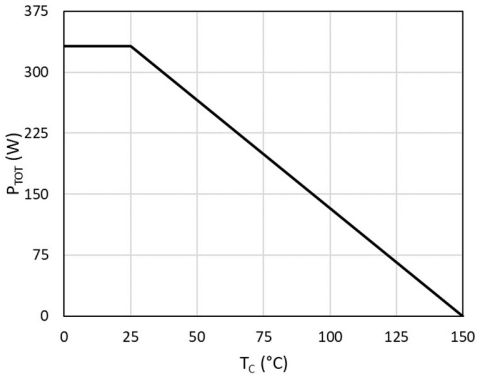


Fig. 12. $P_{DISSIPATION}$ vs. T_{CASE}

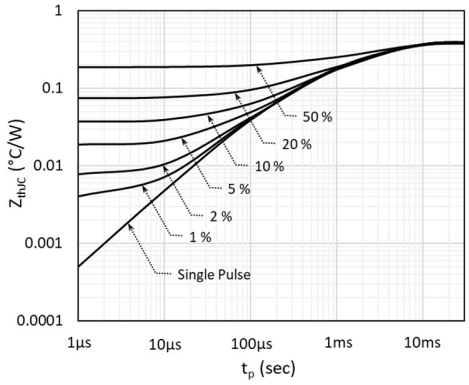


Fig. 13. Transient $R_{\Theta\_JUNC\text{-}CASE}$

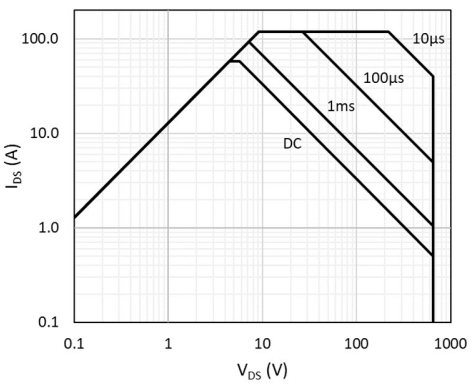


Fig. 14. Safe Operating Area, T_{JUNC} = 25°C

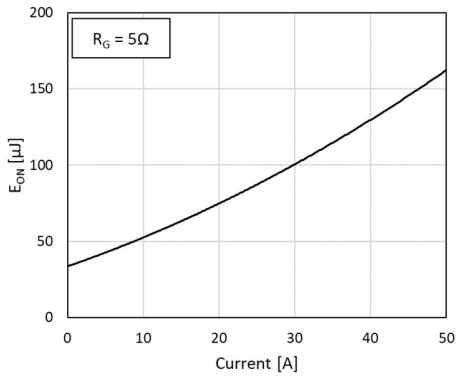


Fig. 15. E_{ON} vs. I_{DS}, T_{JUNC} = 25 °C

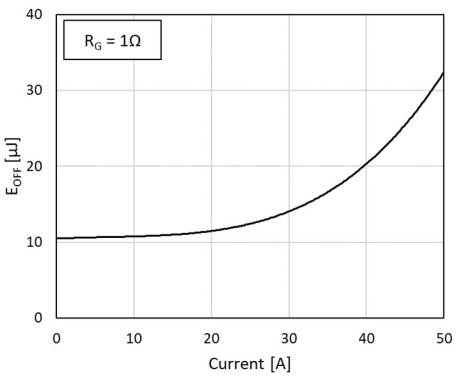


Fig. 16. E_{OFF} vs. I_{DS}, T_{JUNC} = 25 °C

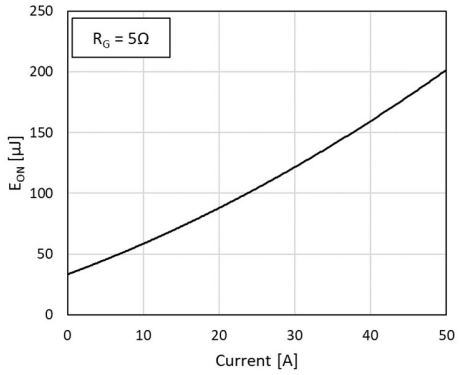


Fig. 17. E_{ON} vs. I_{DS}, T_{JUNC} = 125°C

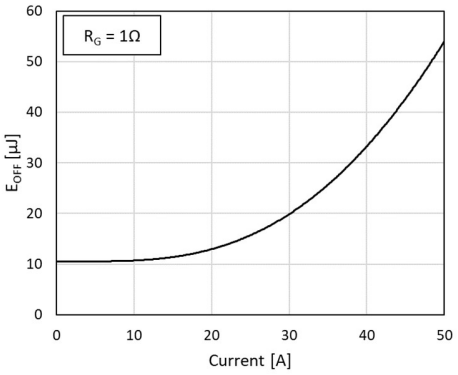


Fig. 18. E_{OFF} vs. I_{DS}, T_{JUNC} = 125°C

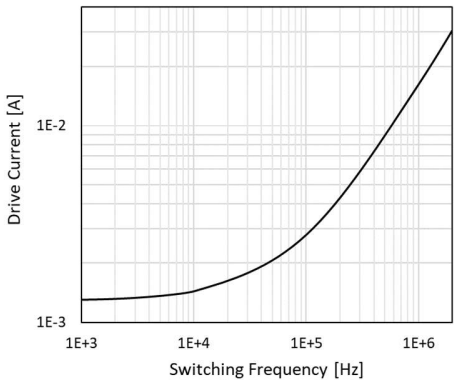
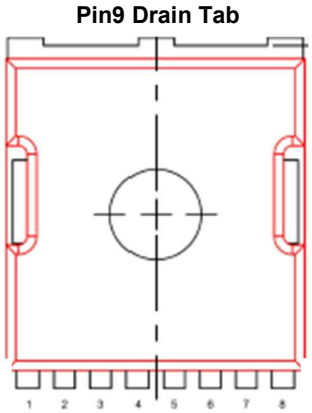


Fig. 19. I_{DRIVE} vs. Switching Frequency (F_{SW})

13. Pinout Table



Pin		I/O (Note 8)	Description
Number	Symbol		
1~6, Bottom Pad	Source	G	Source of power FET
7	SK	G	Connect Driver IC between V_{DRIVE} and SK (Kelvin return)
8	V_{DRIVE}	I	
9 (Tab)	Drain	P	Drain of power FET

(8) G = Ground, I = Input, P = Power

14. Functional Description

14.1. GaNSafe Operation: Internal Regulated V_{GS} and Block Diagram

GaNSafe power IC's are the industry's first GaN power devices allowing high speed operation in an industry-standard 4-Pin package (Drain / Source / V_{DRIVE} / SK) ~ ***also providing regulated V_{GS} and protection & performance features!***

V_{DRIVE} Input: In order to achieve these advanced capabilities in only 4 terminals, an isolated PWM with ≥500mA output current is required (see sect. 14.10 reference schematic). The PWM output (V_{DRIVE} input) must be ≥10V (***absolute minimum***), however, V_{DRIVE} voltage ≥11V is ***strongly recommended***. During normal operation all the GaNSafe internal circuit blocks are active with V_{DRIVE} > 8.5V, however, all functions (dV/dt slew rate over Temp, SCP, etc.) are only guaranteed to meet datasheet parameters with V_{DRIVE} ≥10V (recommended ≥11V).

Internal regulated V_{GS} turns-ON the GaN gate with 6.7V and OFF at 0V. Negative gate bias is NOT required since there is an internal Miller Clamp to maintain the GaN gate OFF during PWM OFF state. The internal regulated V_{GS} has a Positive TempCo (PTC) to optimize V_{GS} over -40C to +150C T_{JUNC}, maintaining V_{GS} close to optimal 6.7V but below 7.0V lifetime reliability constraint. This is part of the overall reliability and robustness provided by GaNSafe.

V_{DS} Rating: During switching, the Drain toggles between Source voltage and V_{IN} (650V maximum). The Drain can withstand ***non-repetitive*** pulses up to 800V for <100 us [see sect. 6 for $V_{DS(TRAN)}$ rating]. The platform design must have appropriate commutation loop decoupling and adhere to voltage margin.

PWM IC: A dual PWM driver can be utilized (sect. 14.10 reference schematic), or a single PWM driver with separate Turn-ON and Turn-OFF outputs can be used, such as Si8273BB with 8V UVLO.

Minimum On-Time: GaNSafe power ICs have an integrated 5V power supply and Level Shift & Deglitch circuits. The t_{ON_MIN} (minimum valid on-time pulse duration at the V_{DRIVE} pin) is 75ns (sect. 10).

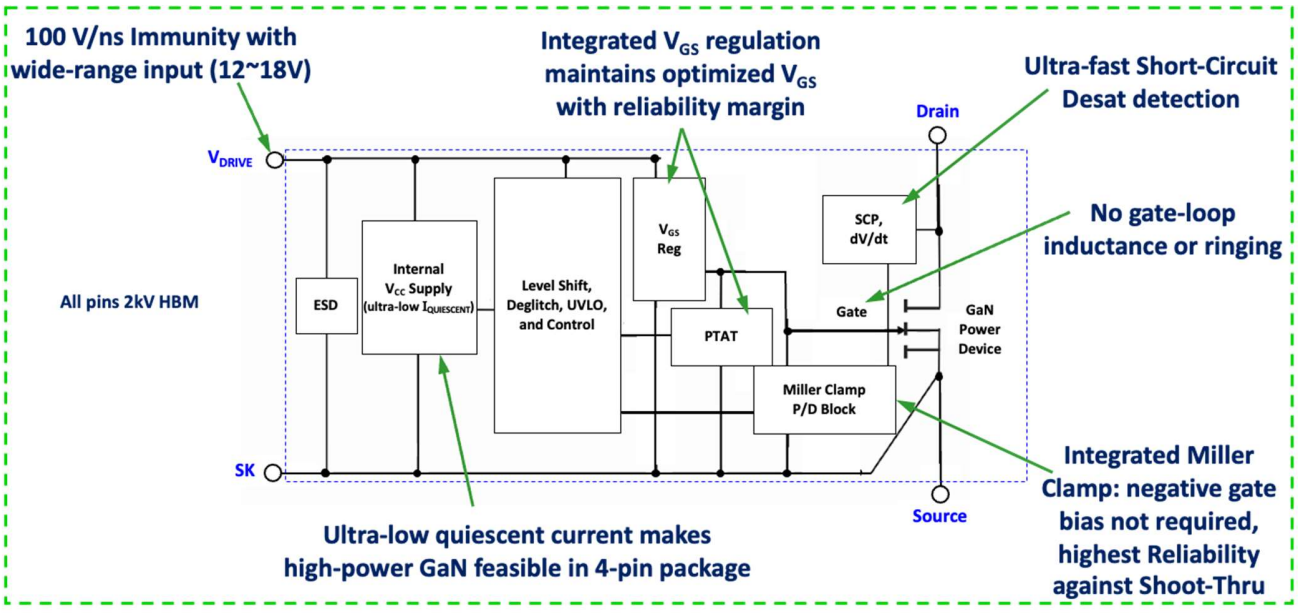


Figure 20. GaNSafe Block Diagram

14.2. Internal Gate Drive Power Loss

Internal gate drive power loss on GaNSafe power IC's can be projected by using I_{DRIVE} value from Fig. 19 (I_{DRIVE} vs. F_{SW}), interpolated between duty cycle curves, multiplied by V_{DRIVE} (i.e., I_{DRIVE} * V_{DRIVE}).

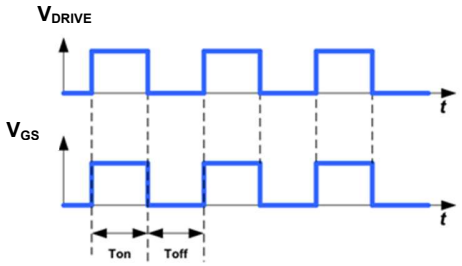


Figure 21. Normal Operating Mode Timing Diagram (V_{DRIVE} input vs. V_{GS})

14.3. Programmable Turn-ON and Turn-OFF dV/dt Control

During start-up or hard-switching condition, it may be desirable to limit slew rate (dV/dt) on the Drain. To program Turn-ON slew rate connect R_{DRIVE_ON} in series with V_{DRIVE} pin (as shown in sect. 14.10 reference schematic). Conversely, Turn-OFF slew rate is programmed using R_{DRIVE_OFF} series resistor value. These resistors ($R_{DRIVE\_ON, OFF}$) set the ***current*** of the internal gate drive circuit, therefore setting dV/dt.

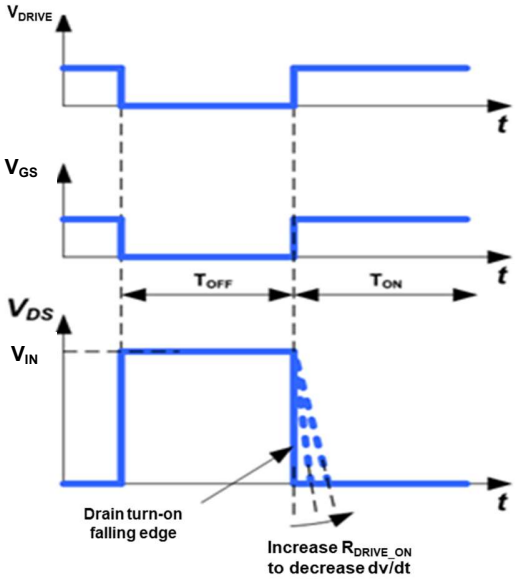


Figure 22. Turn-on dV/dt Slew Rate Control

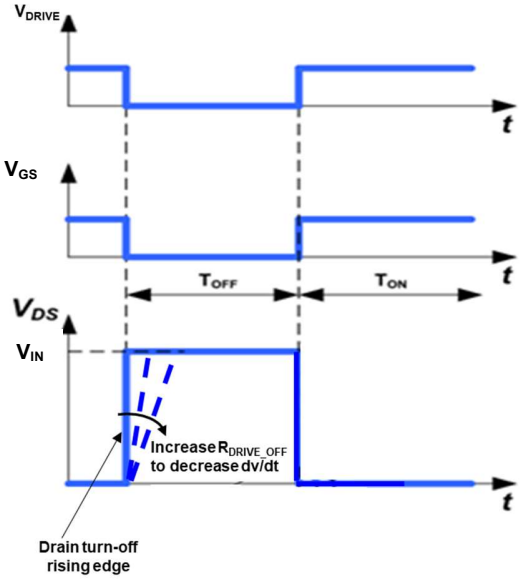


Figure 23. Turn-OFF dV/dt Slew Rate Control

14.4. Paralleling GaNSafe power IC's

GaNSafe power IC's can be paralleled up to a recommended maximum of **Qty2**, maintaining close T_{ON} and T_{OFF} matching of propagation delays. The following schematic revisions should be made:

- Add Kelvin-Source resistors in the return path from ***each*** SK Pin back to the external isolated PWM driver
- Adjust R_{DRIVE} value to assist T_{ON} / T_{OFF} matching

14.5. Short Circuit Protection

GaNSafe power ICs continuously monitor V_{DS} and trigger Short Circuit Protection (SCP) above V_{DS_SAT} trip point (listed in sect. 10). GaNSafe power ICs Turn-OFF via Soft Shutdown (S/D) after SCP is triggered, holding the GaN gate LOW on a cycle-by-cycle basis unless V_{DS_SAT} setpoint is CLEARED or until the system undergoes Power-ON Reset (POR).

V_{DS_SAT} Min/Max tolerances (listed in sect. 10) are designed to set SCP trip point $\geq$20% higher than the GaN power device saturation current, up to 150C. SCP latency is 350ns including Blanking Time during Turn-ON ***into*** a short circuit event, but SCP latency is 50ns when a short circuit event occurs during normal switching operation.

It is critical for GaN devices to have integrated SCP (Short Circuit Protection) due to GaN's shorter SCWT (Short Circuit Withstand Time) and the need for ultra-low latency on SCP operation. However, OTP (Over Temp) & OCP (Over Current) are typically implemented via system DSP.

14.6. Design for $V_{DS(CONT)}$ and $V_{DS(TRAN)}$

GaNSafe power ICs have been designed and tested to provide significant design margin for continuous and transient voltage conditions, for topologies typically used in high power operation up to 22kW. These voltage levels and recommended design margin can be analyzed using Fig. 24 below. When the GaNSafe power IC is switched off, energy stored in the output circuit causes V_{DS} overshoot (V_{SPIKE}), and after dissipation of the stored energy V_{DS} settles to the level of the bus voltage.

- For ***repetitive*** events, derating should be applied from $V_{DS(TRAN)}$ rating (800V) to $V_{DS(CONT)}$ rating (650V max) under the worst case operating conditions.
- It is recommended to design the system such that V_{DS-OFF} is $\leq$ 520V (80% of $V_{DS(CONT)}$ rating).
- ***Non-repetitive events*** are infrequent, ***one-time*** conditions such as line surge, ESD, and lightning strike. No derating from 800V is needed for non-repetitive V_{SPIKE} durations < 100 µs.

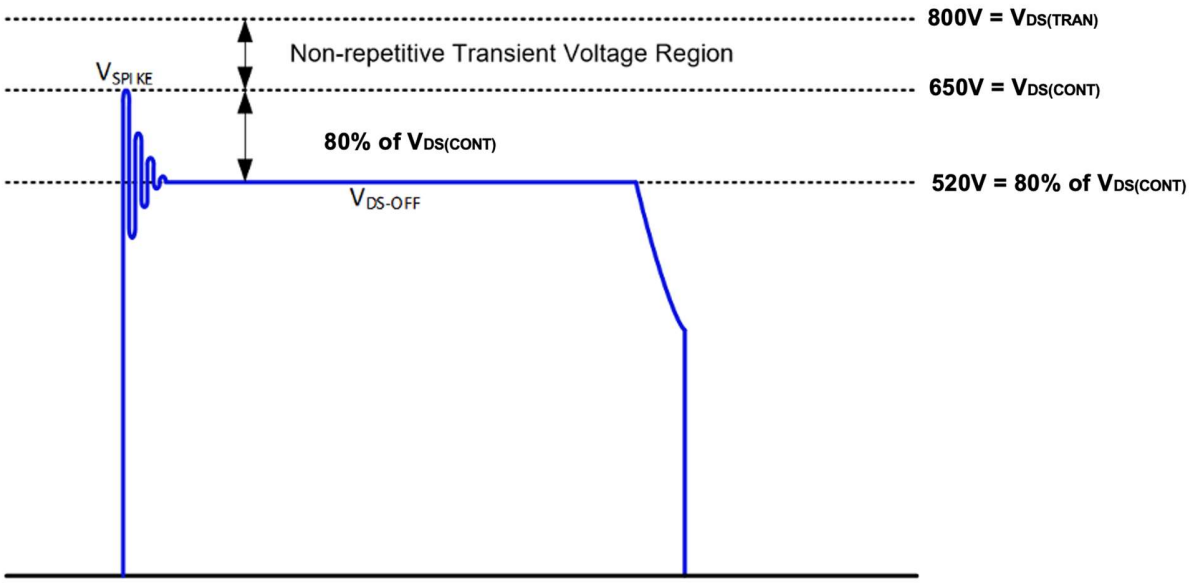


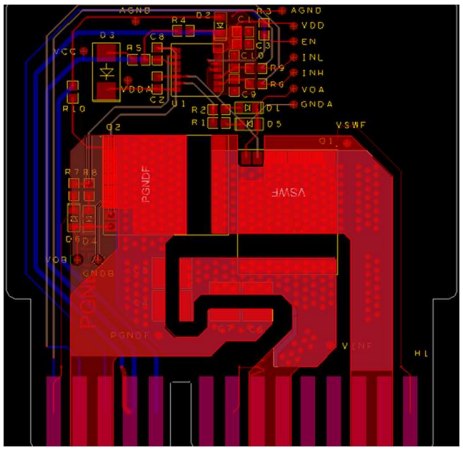
Figure 24. $V_{DS(CONT)}$ and $V_{DS(TRAN)}$

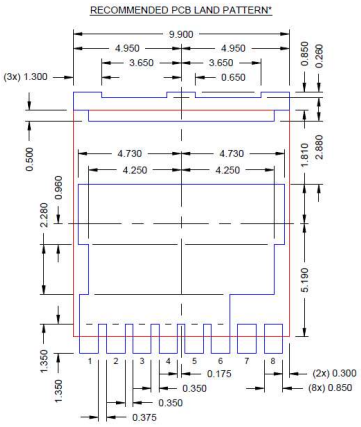
14.7. PCB Layout Guidelines

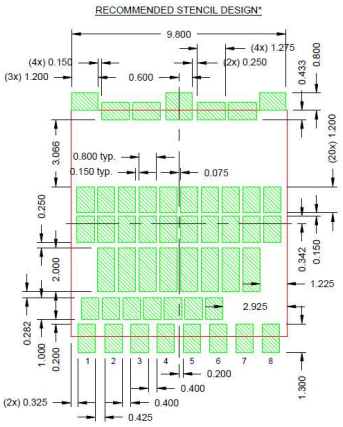
PCB layout is critical for thermal management, noise immunity, and proper operation of the power IC. The following rules should be followed carefully during the design of the PCB layout:

- Place IC filter and programming components **directly adjacent to the GaNSafe power IC**, and reference all these components to the SK pin.
- Place an 0402 site for MLCC between SK and V_{DRIVE} Pins (**directly adjacent to the pins**). This site may be stuffed with a 100pF MLCC if additional noise immunity on V_{DRIVE} Pin is desired.
- Observe the limits on **R_{DRIVE_ON} and R_{DRIVE_OFF} minimum values** in ROC Sect. 7.
- Do ***not*** run power SOURCE currents through SK pin!
- For best thermal management, place thermal vias in the source pad area to conduct the heat out through the bottom of the package and through the PCB board to other layers.
- Use large PCB thermal planes (connected with thermal vias to the source pad) and additional PCB layers to reduce IC temperatures as much as possible.

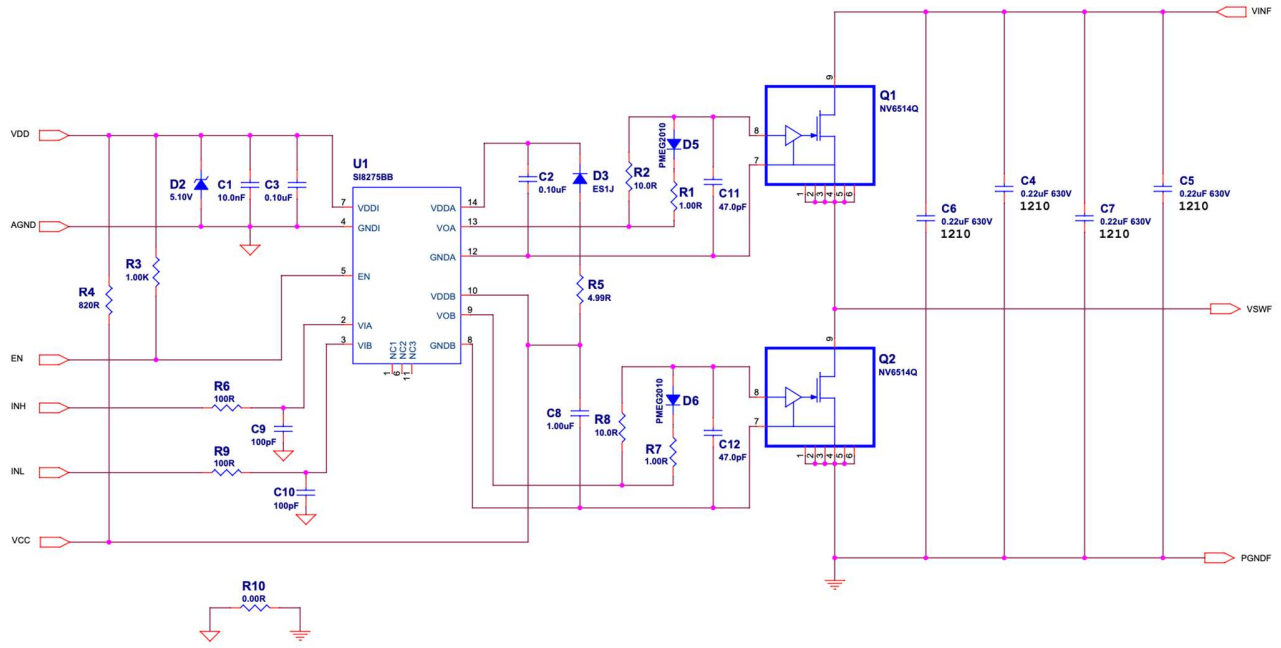
Pictorials below shows a typical Half-Bridge layout from a THMT Eval Board, and PCBA Footprint.



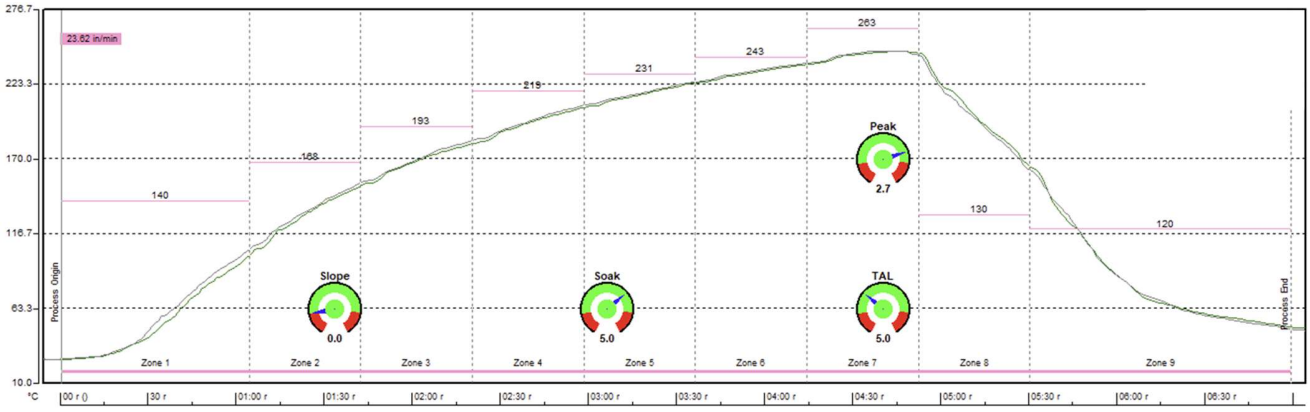




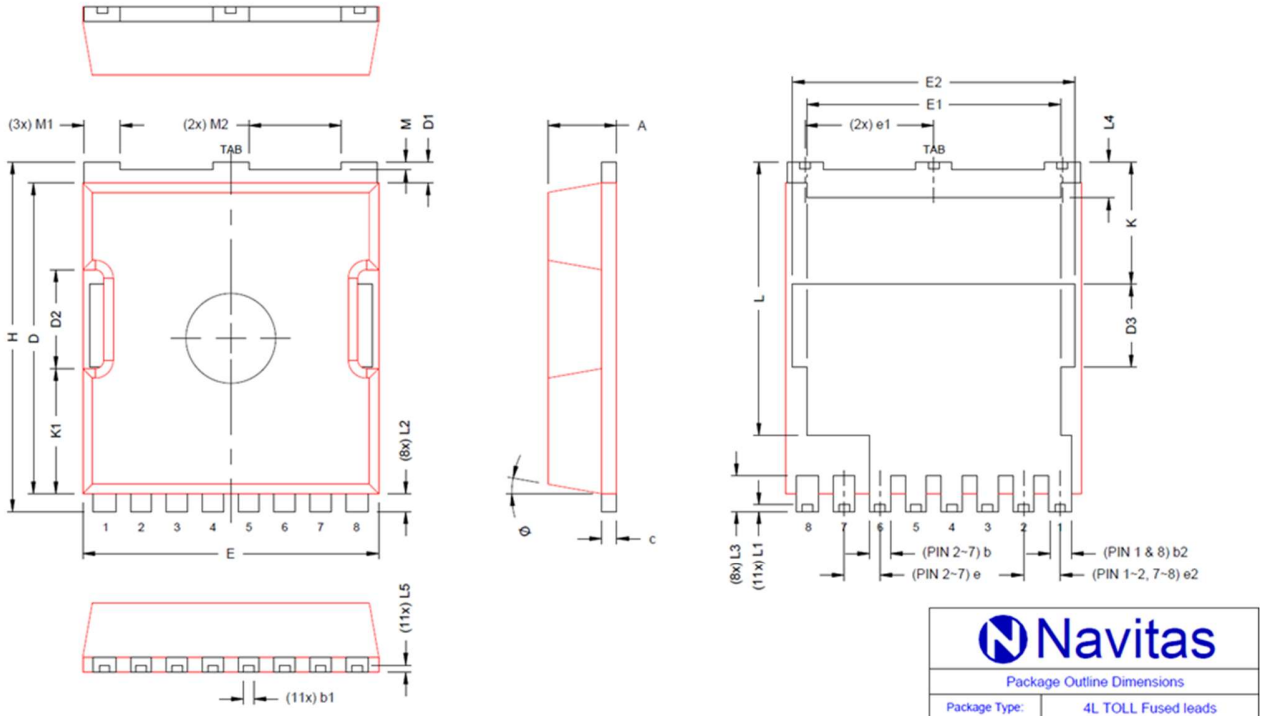
14.8. Reference Schematic



14.9. PCBA SMT IR Oven Profile (*guideline only*):



15. Package Outline Dimensions:



NOTES:

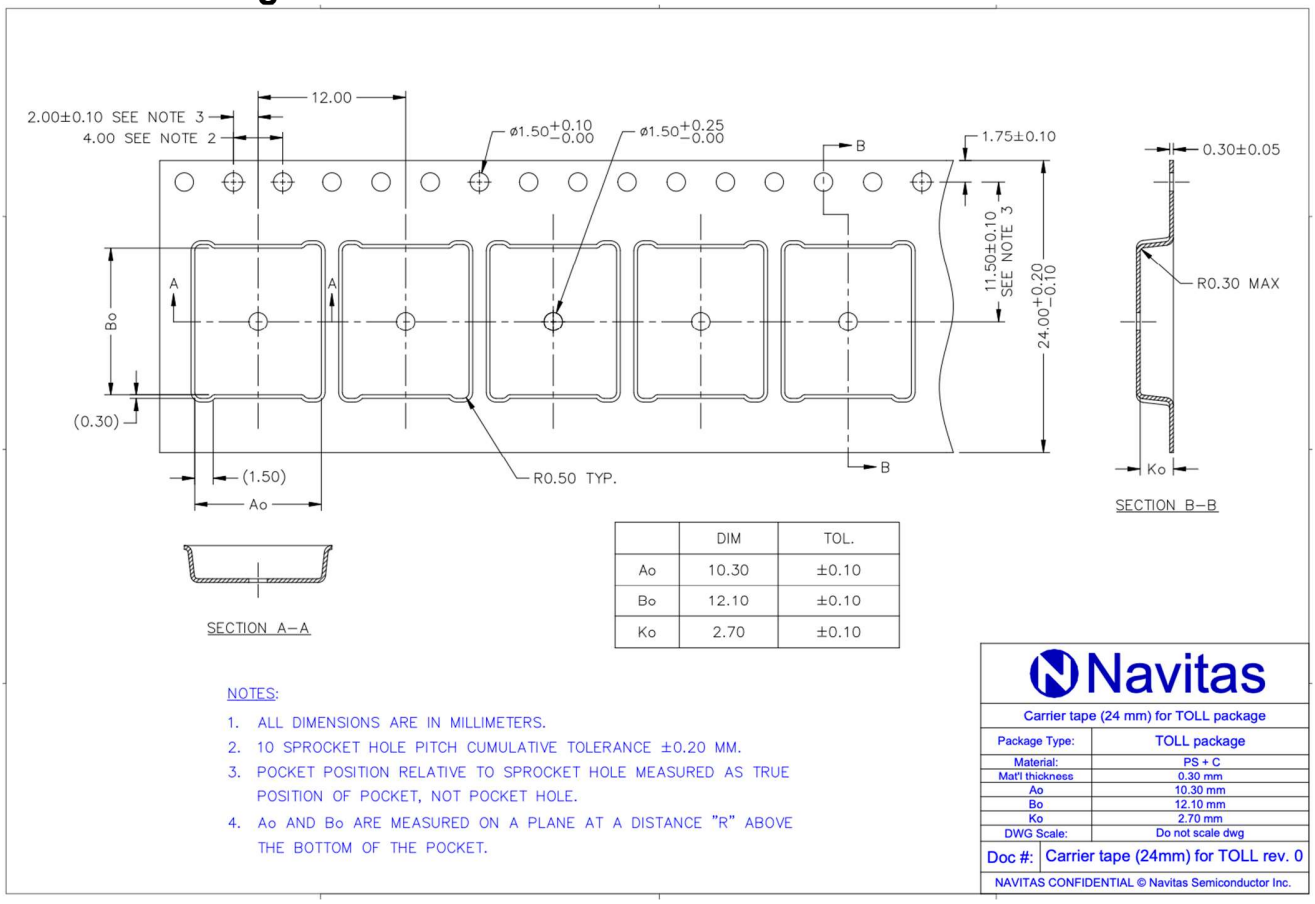
1. DIMENSIONING AND TOLERANCING CONFORME TO ASME Y14.5M – 1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. MAXIMUM ALLOWABLE BURRS IS 0.076 MM IN ALL DIRECTIONS.
4. COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SLUG AS WELL AS THE TERMINALS.

Navitas

Package Outline Dimensions	
Package Type:	4L TOLL Fused leads
Lead Count:	8
Body X:	9.90 mm
Body Y:	10.38 mm
Body Z:	2.30 mm
LF Type:	Selective Ag plated LF
DWG Scale:	Do not scale dwg
Doc #:	4L TOLL Fused Leads

SYM	MIN	NOM	MAX
A	2.15	2.30	2.45
b	0.70	0.70	0.80
b1	–	0.35 REF.	–
b2	0.75	0.75	0.85
c	0.40	0.50	0.60
D	10.18	10.38	10.58
D1	0.50	0.70	0.90
D2	–	3.30 REF.	–
D3	–	2.77 REF.	–
E	9.70	9.90	10.10
E1	–	8.50 REF	–
E2	–	9.46 REF.	–
e	1.15	1.20	1.25
e1	4.20	4.30	4.40
e2	1.175	1.225	1.275
H	11.48	11.68	11.88
K	–	4.08 REF.	–
K1	–	4.17 REF.	–
L	–	9.13 REF.	–
L1	–	0.23 REF.	–
L2	0.50	0.60	0.70
L3	1.10	1.20	1.30
L4	1.10	1.20	1.30
L5	–	0.23 REF.	–
M	0.16	0.26	0.36
M1	1.10	1.20	1.30
M2	3.00	3.10	3.20
Ø	8°	10°	12°

16. TnR Drawing and Socket Orientation



	DIM	TOL.
Ao	10.30	±0.10
Bo	12.10	±0.10
Ko	2.70	±0.10

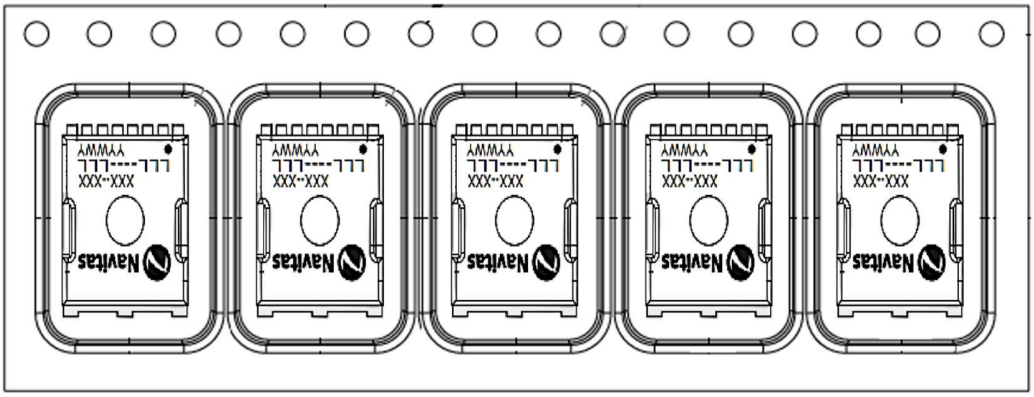
NOTES:

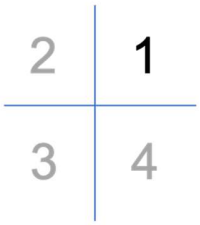
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. 10 SPROCKET HOLE PITCH CUMULATIVE TOLERANCE ±0.20 MM.
3. POCKET POSITION RELATIVE TO SPROCKET HOLE MEASURED AS TRUE POSITION OF POCKET, NOT POCKET HOLE.
4. Ao AND Bo ARE MEASURED ON A PLANE AT A DISTANCE "R" ABOVE THE BOTTOM OF THE POCKET.

Navitas

Carrier tape (24 mm) for TOLL package

Package Type:	TOLL package
Material:	PS + C
Mat'l thickness	0.30 mm
Ao	10.30 mm
Bo	12.10 mm
Ko	2.70 mm
DWG Scale:	Do not scale dwg
Doc #:	Carrier tape (24mm) for TOLL rev. 0





17. Ordering Information

Part Number	Qualification	Package	MSL Rating	TnR Sizes/Qtys
NV6515	JEDEC	TOLL-4L Bottom-cooled SMD	3	Standard (13” dia) Qty1,500
NV6515-MR				Mini-Reel (7” dia) Qty340
NV6515Q	AEC-Q100 Grade 1 -40 °C to +125 °C			Standard (13” dia) Qty1,500
NV6515Q-MR				Mini-Reel (7” dia) Qty340

18. Revision History

Date	Status	Notes
Oct 20th, 2022	Initial Publication	• Preliminary Datasheet
Feb 1st, 2023 and Apr 20th, 2023	Revisions	• Updated electrical characteristics table • Added reference schematic
Oct 6th, 2023	Revision	• Absolute Maximum Ratings: V_{DRIVE_TRANS} (transient) • ROC table: Turn-ON/OFF R_{DRIVE} series resistor values • Electrical Characteristics table: $t_{ON/OFF}$ and t_{PROP_DELAY} Min/Max values with Test Conditions ; I_{SD} Typ value ; SCP parameters V_{DS_SCP} trip point and delay times ; (all) Switching Parameters • Electrical curves (all) updated from FT Characterization data • Applications: 14.3 updated ; 14.6 added ; 14.7 & 14.8 updated • TnR DWG and Socket Orientation DWG added
Jan 12th, 2024	Revision	• Electrical Characteristics table: $V_{DRIVE\_OPERATING}$, $V_{DRIVE\_LEAKAGE}$, $t_{ON/OFF}$, V_{DS_SCP}, $I_{DSS\_25°C}$, $I_{DSS\_150°C}$, V_{SD}, I_{SD_PULSED}, $C_{O(TR)}$, $E_{ON/OFF}$ • Updated Figures 11 – 19 • Added Sect. 14.6

Additional Information

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