GaNFast™ Power IC
with GaNSense™ Technology

1. Features

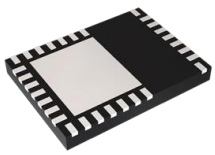
GaNFast™ Power IC
- Monolithically-integrated gate drive
- Wide V_{CC} range (10 to 30 V)
- Programmable turn-on dV/dt
- 200 V/ns dV/dt immunity
- 800 V Transient Voltage Rating
- 700 V Continuous Voltage Rating
- Low 120 mΩ resistance
- Zero reverse recovery charge
- 2 MHz operation

GaNSense™ Technology
- Integrated loss-less current sensing
- Short-circuit protection
- Over-temperature protection
- Autonomous low-current standby mode
- Auto-standby mode input

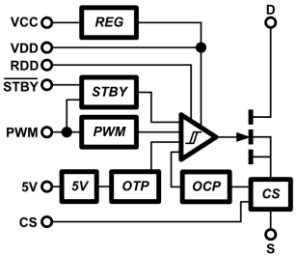
Small, low-profile SMT QFN
- 6 x 8 mm footprint, 0.85 mm profile
- Minimized package inductance
- Large cooling pad

Sustainability
- RoHS, Pb-free, REACH-compliant
- Up to 40% energy savings vs Si solutions
- System level 4kg CO_2 Carbon Footprint reduction

Product Reliability
- 20-year limited product warranty (see Section 14 for details)



QFN 6 x 8 mm



Simplified schematic

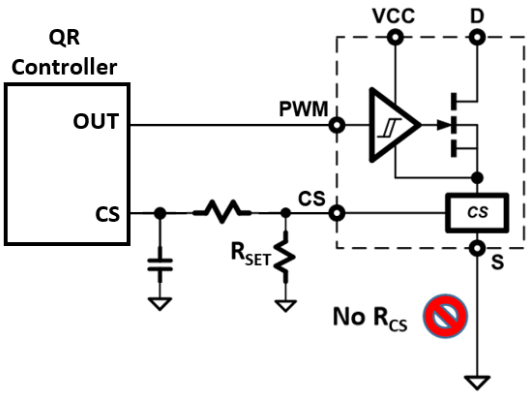
2. Topologies / Applications
- AC-DC, DC-DC, DC-AC
- QR flyback, Class D, PFC
- Wireless power, Solar Micro-inverters
- LED lighting, TV SMPS, Server, Telecom

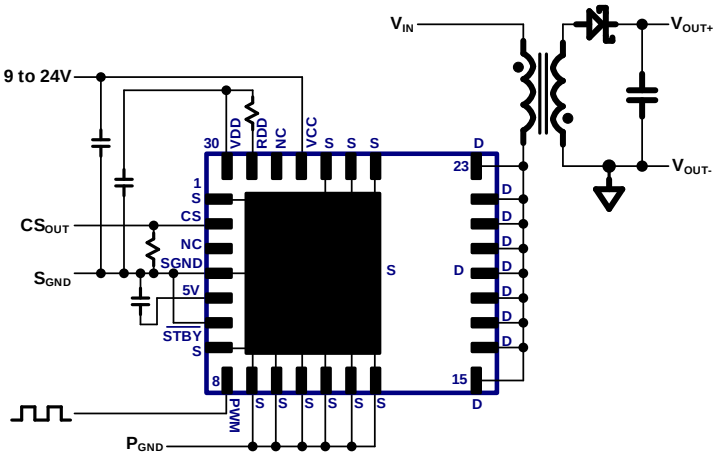
3. Description

This GaNFast™ power IC integrates a high performance eMode GaN FET with integrated gate drive to achieve unprecedented high-frequency and high efficiency operation. GaNSense™ technology is also integrated which enables real-time, accurate sensing of voltage, current and temperature to further improve performance and robustness not achieved by any discrete GaN or discrete silicon device. GaNSense™ enables integrated loss-less current sensing which eliminates external current sensing resistors and increases system efficiency. GaNSense™ also enables short circuit and over-temperature protection to increase system robustness, while auto-standby mode increases light, tiny & no-load efficiency. These GaN ICs combine the highest dV/dt immunity, high-speed integrated drive and industry-standard low-profile, low-inductance, SMT QFN packaging to enable designers to achieve simple, quick and reliable solutions. Navitas' GaN IC technology extends the capabilities of traditional topologies such as flyback, PFC, buck/boost, and other converters to reach MHz+ frequencies with very high efficiencies and low EMI to achieve unprecedented power densities at a very attractive cost structure.

4. Typical Application Circuits

Loss-less Current Sensing





HF QR Flyback

5. Table of Contents

6. Specifications

6.1. Absolute Maximum Ratings(1)

(with respect to Source (pad) unless noted)

SYMBOL	PARAMETER	MAX	UNITS
$V_{DS\ (CONT)}$	Drain-to-Source Voltage	-7 to +700	V
$V_{DS\ (TRAN)}$	Transient Drain-to-Source Voltage(2)	800	V
V_{CC}	Supply Voltage	30	V
V_{DD}	Drive Supply Voltage	7.8	V
R_{DD}	Input Voltage	7.8	V
$V_{\overline{STBY}}$	Auto-Standby Mode Pin Voltage	-0.6 to +20 or V_{CC}	V
V_{5V}	5 V Pin Voltage	6	V
V_{PWM}	PWM Input Pin Voltage	-0.6 to +20 or V_{CC}	V
V_{CS}	CS Pin Voltage	5.3	V
I_D	Continuous Drain Current (@ T_C = 100ºC)	8.6	A
I_D PULSE	Pulsed Drain Current (10 µs @ T_J = 25ºC)	17.2	A
dV/dt	Slew Rate	200	V/ns
T_J	Junction Temperature	-55 to 150	ºC
T_{STOR}	Storage Temperature	-55 to 150	ºC

(1) Absolute maximum ratings are stress ratings; devices subjected to stresses beyond these ratings may cause permanent damage.

(2) $V_{DS\ (TRAN)}$ rating allows for surge ratings during non-repetitive events that are <100us (for example start-up, line interruption). $V_{DS\ (TRAN)}$ rating allows for repetitive events that are <400ns, with 80% derating required (for example repetitive leakage inductance spikes). Refer to Section 8.9 for detailed recommended design guidelines.

6.2. Recommended Operating Conditions(3)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
V_{CC}	Supply Voltage	9		24	V
V_{PWM}	PWM Input Pin Voltage	0	5	15 or V_{CC}	V
$V_{\overline{STBY}}$	Auto-Standby Mode Pin Voltage	0	5	15 or V_{CC}	V
R_{DD}	Gate drive turn-on current set resistor	10	50		Ω
T_J	Operating Junction Temperature	-40		125	ºC

(3) Exposure to conditions beyond maximum recommended operating conditions for extended periods of time may affect device reliability.

6.3. ESD Ratings

SYMBOL	PARAMETER	MAX	UNITS
HBM	Human Body Model (per JESD22-A114)	2,000	V
CDM	Charged Device Model (per JESD22-C101F)	1,000	V

6.4. Thermal Resistance

SYMBOL	PARAMETER	TYP	UNITS
$R_{\theta JC}$ (4)	Junction-to-Case	1.5	ºC/W
$R_{\theta JA}$ (4)	Junction-to-Ambient	40	ºC/W

(4) R_θ measured on DUT mounted on 1 square inch 2 oz Cu (FR4 PCB)

6.5. Electrical Characteristics

Typical conditions: V_{DS}=400V, V_{CC} =15V, F_{SW}=1MHz, T_{AMB}=25ºC, I_D=4.3A (unless otherwise specified)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
VCC & V_{DD} Supply Characteristics						
V_{CCUV+}	V_{CC} UVLO Rising Turn-On Threshold	8	8.4	9.3	V	
V_{CCUV-}	V_{CC} UVLO Falling Turn-Off Threshold		7.3		V	
$I_{QCC-STBY}$	V_{CC} Standby Current		235		µA	$\overline{STBY}$ = 0 V
I_{QCC}	V_{CC} Quiescent Current		0.53	0.8	mA	V_{PWM} = 0 V, $\overline{STBY}$ = 5 V OR V_{PWM} = 5 V, $\overline{STBY}$ = 0 V
I_{QCC-SW}	V_{CC} Operating Current		2.9		mA	F_{SW} = 1 MHz, V_{DS} = Open
V_{DD}	V_{DD} Supply Voltage	6.3	6.8	7.2	V	V_{CC} = 15 V, V_{PWM} = 0 V $\overline{STBY}$= 5 V
5V Output (5V pin)						
V_{5V}	5V Output Voltage	4.4	5	5.5	V	$\overline{STBY}$= 5 V
Input Logic Characteristics (PWM, $\overline{STBY}$)						
$V_{LOGIC-H}$	Input Logic High Threshold (rising edge)		2.5	2.8	V	
$V_{LOGIC-L}$	Input Logic Low Threshold (falling edge)	1.1	1.2		V	
$V_{LOGIC-HYS}$	Input Logic Hysteresis		1.3		V	
Switching Characteristics						
F_{SW}	Switching Frequency			2	MHz	R_{DD} = 10 Ω
t_{PW}	Pulse width	30			ns	
T_{ON}	Turn-on Propagation Delay		29.6		ns	Fig 1
T_{OFF}	Turn-off Propagation Delay		23.8		ns	Fig 1
T_R	Drain rise time		6.9		ns	Fig 1
T_F	Drain fall time		5.2		ns	Fig 1

6.6. Electrical Characteristics (2, cont.)

Typical conditions: V_{DS}=400V, V_{CC} =15V, F_{SW}=1MHz, T_{AMB}=25ºC, I_D=4.3A (unless otherwise specified)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
Current Sense Characteristics (CS pin)						
I_{CS}	CS Pin Output Current	1.16	1.25	1.34	mA	V_{PWM} = 5 V, I_{DS} = 6.21 A
Offset	CS Output Offset		+18		µA	V_{PWM} = 5 V, I_{DS} = 0 A
t_{CSDLY}	CS Pin Delay (from I_{DS} to V_{CS}, at 10% rated current)		55		ns	di/dt = 40 A/us, R_{SET} = 400 Ohm, C_{CS} = 25 pF
Over-Current Protection						
OCP_{TH}	OCP Threshold Voltage (V_{CS} Pin)		1.9		V	
Standby Mode Characteristics						
t_{TO_STBY}	Time Out Delay to Enter Standby Mode		90		µs	V_{PWM} = 0 V
t_{ON_FP}	First Pulse Propagation Delay		30		ns	V_{PWM} = 5 V pulse, $\overline{STBY}$ = 0 V
Over-Temperature Protection						
T_{OTP+}	OTP Shutdown Threshold		165		ºC	
T_{OTP_HYS}	OTP Restart Hysteresis		60		ºC	

6.7. Electrical Characteristics (3, cont.)

Typical conditions: V_{DS}=400V, V_{CC} =15V, F_{SW}=1MHz, T_{AMB}=25ºC, I_D=4.3A (unless otherwise specified)

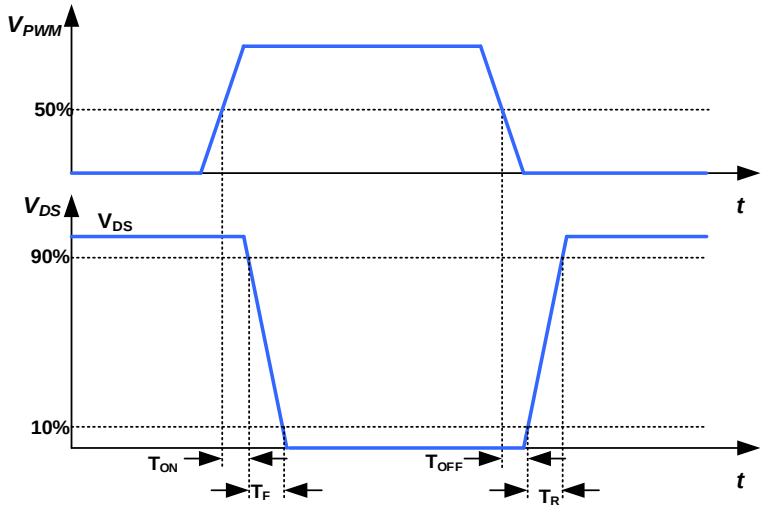
SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
GaN FET Characteristics						
I_{DSS}	Drain-Source Leakage Current		0.51	25	µA	V_{DS} = 700 V, V_{PWM} = 0 V
I_{DSS}	Drain-Source Leakage Current, TC =150 ºC		32		µA	V_{DS} =700V, V_{PWM} =0V, T_C =150 ºC
$R_{DS(ON)}$	Drain-Source Resistance		120	168	mΩ	V_{PWM} = 5 V, I_D = 4.3 A
V_{SD}	Source-Drain Reverse Voltage		3.5	5	V	V_{PWM} = 0 V, I_{SD} = 4.3 A
Q_{OSS}	Output Charge		20.5		nC	
Q_{RR}	Reverse Recovery Charge		0		nC	
C_{OSS}	Output Capacitance		30.17		pF	V_{DS} = 400 V, V_{PWM} = 0 V
$C_{O(er)}$ (Note 1)	Effective Output Capacitance, Energy Related		36.65		pF	V_{DS} = 400 V, V_{PWM} = 0 V
$C_{O(tr)}$ (Note 2)	Effective Output Capacitance, Time Related		51.24		pF	V_{DS} = 400 V, V_{PWM} = 0 V

(Note 1): *$C_{O(er)}$ is a fixed capacitance that gives the same stored energy as C_{OSS} while V_{DS} is rising from 0 to 400 V*

(Note 2): *$C_{O(tr)}$ is a fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 400 V*

6.8. Switching Waveforms

(T_C = 25 ºC unless otherwise specified)



6.9. Characteristic Graphs

(GaN FET, T_C = 25 ºC unless otherwise specified)

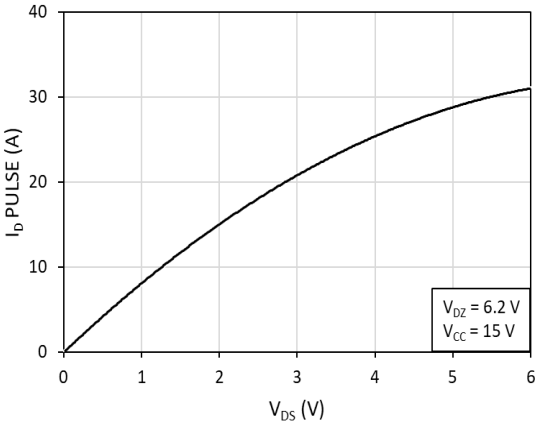


Fig. 2. Pulsed Drain current (I_D PULSE) vs. drain-to-source voltage (V_{DS}) at T = 25 °C

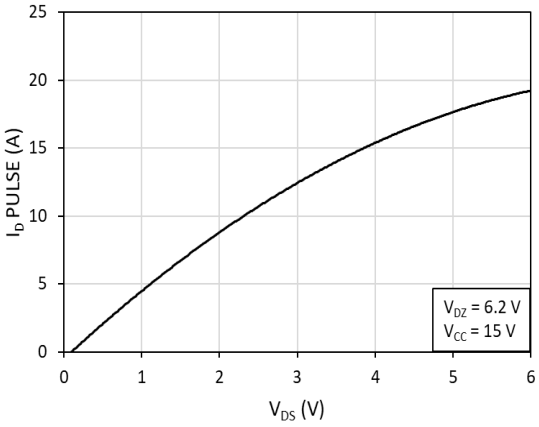


Fig. 3. Pulsed Drain current (I_D PULSE) vs. drain-to-source voltage (V_{DS}) at T = 125 °C

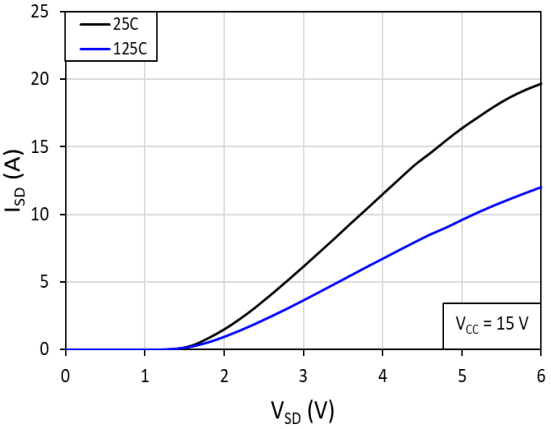


Fig. 4. Source-to-drain reverse conduction voltage

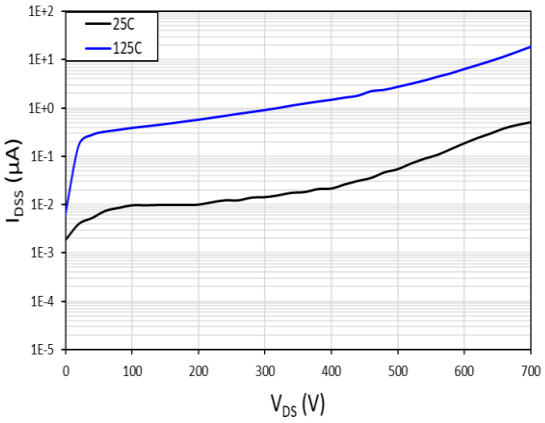


Fig. 5. Drain-to-source leakage current (I_{DSS}) vs. drain-to-source voltage (V_{DS})

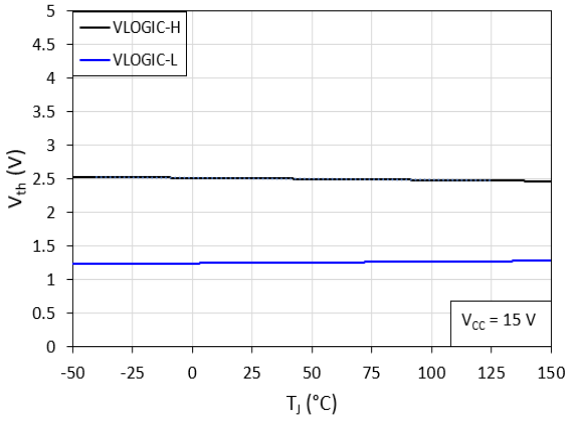


Fig. 6. $V_{LOGIC-H}$ and $V_{LOGIC-L}$ vs. junction temperature (T_J)

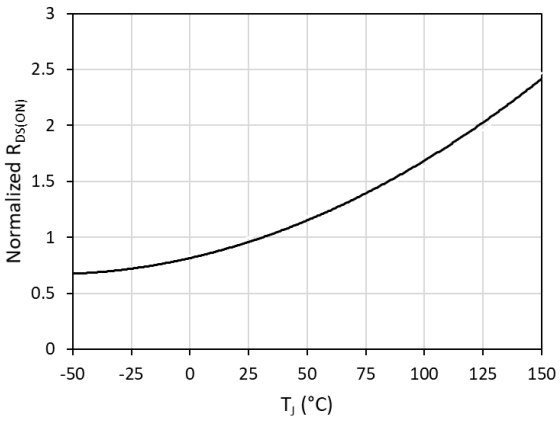


Fig. 7. Normalized on-resistance ($R_{DS(ON)}$) vs. junction temperature (T_J)

Characteristic Graphs (Cont.)

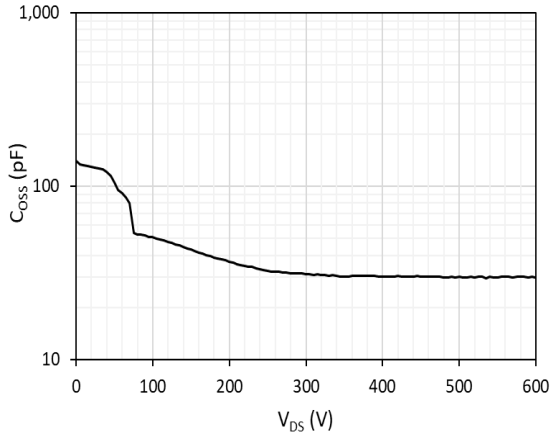


Fig. 8. Output capacitance (C_{OSS}) vs. drain-to-source voltage (V_{DS})

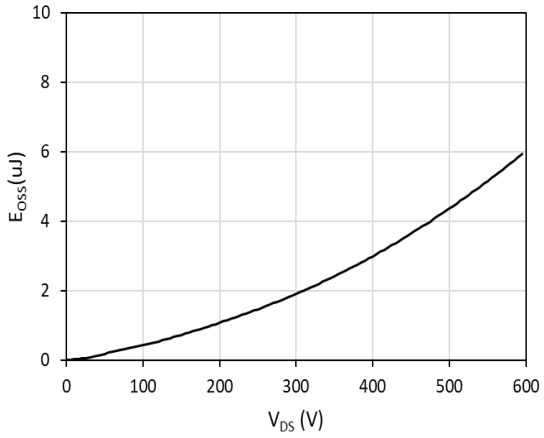


Fig. 9. Energy stored in output capacitance (E_{OSS}) vs. drain-to-source voltage (V_{DS})

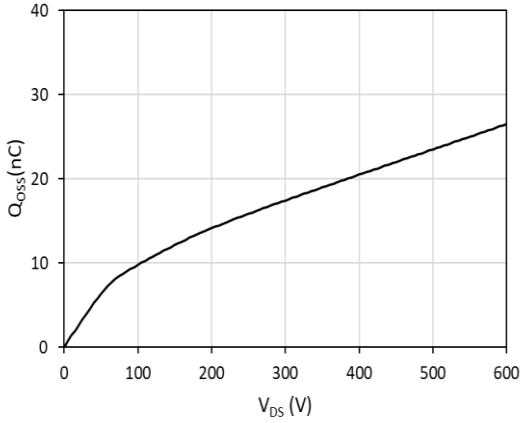


Fig. 10. Charge stored in output capacitance (Q_{OSS}) vs. drain-to-source voltage (V_{DS})

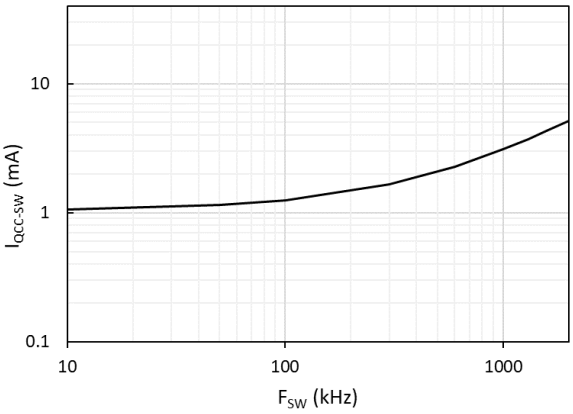


Fig. 11. V_{CC} operating current (I_{QCC-SW}) vs. operating frequency (F_{SW})

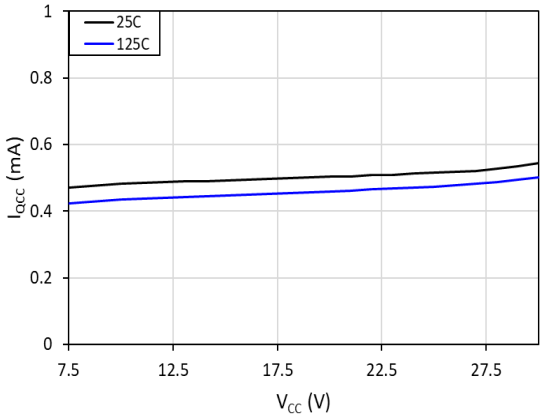


Fig. 12. V_{CC} quiescent current (I_{QCC}) vs. supply voltage (V_{CC})

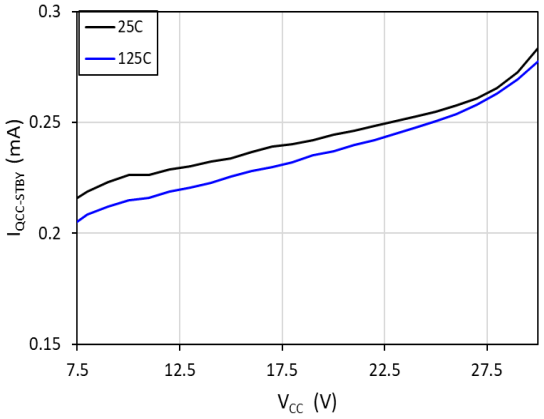


Fig. 13. V_{CC} stand-by quiescent current (I_{QCC}) vs. supply voltage (V_{CC})

Characteristic Graphs (Cont.)

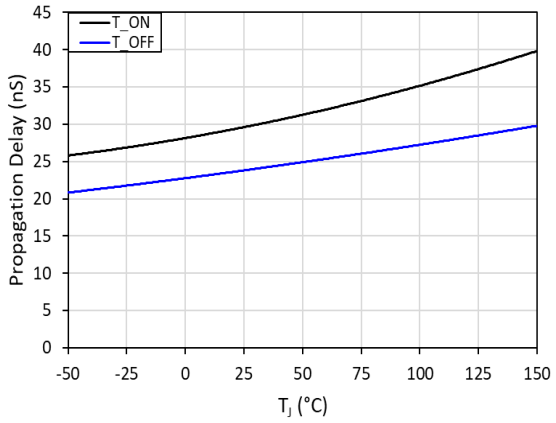


Fig. 14. Propagation delay (T_{ON} and T_{OFF}) vs. junction temperature(T_J)

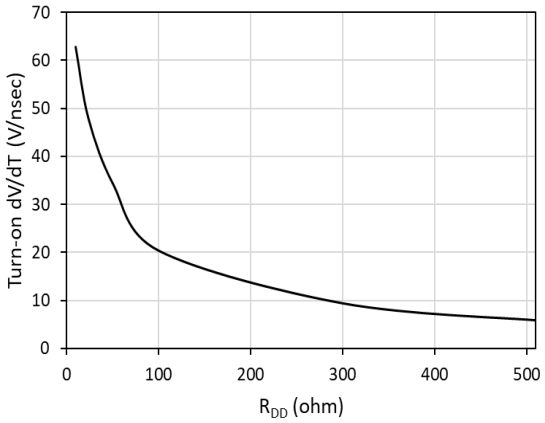


Fig. 15. Slew rate (dV/dt) vs. gate drive turn-on current set resistance (R_{DD}) at T = 25 °C

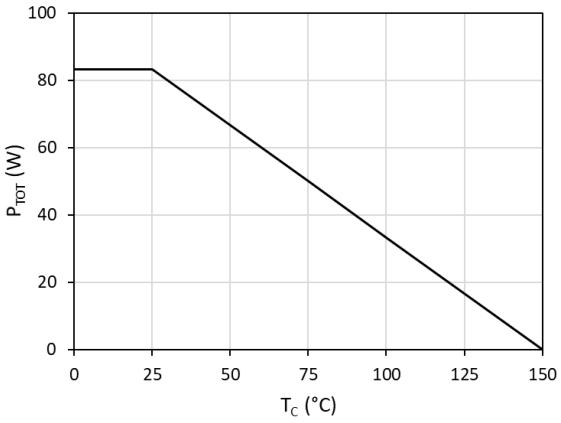


Fig. 16. Power dissipation (P_{TOT}) vs. case temperature (T_C)

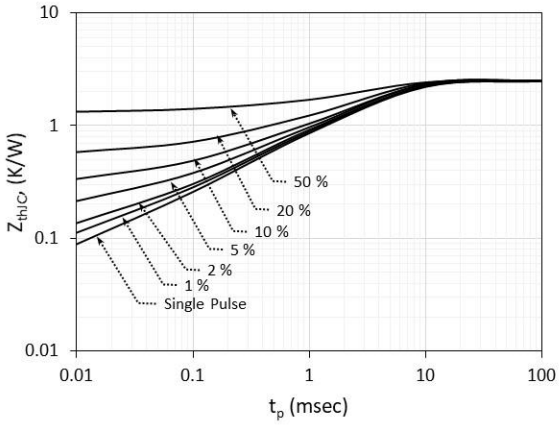


Fig. 17. Max. thermal transient impedance (Z_{thJC}) vs. pulse width (t_P)

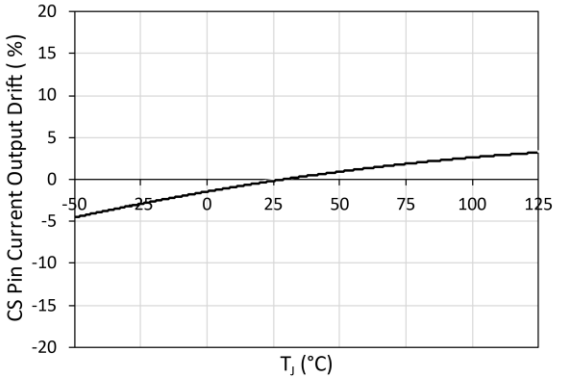


Fig. 18. CS Pin Current Output Drift vs. case temperature (T_C)

7. Pin Configurations and Functions

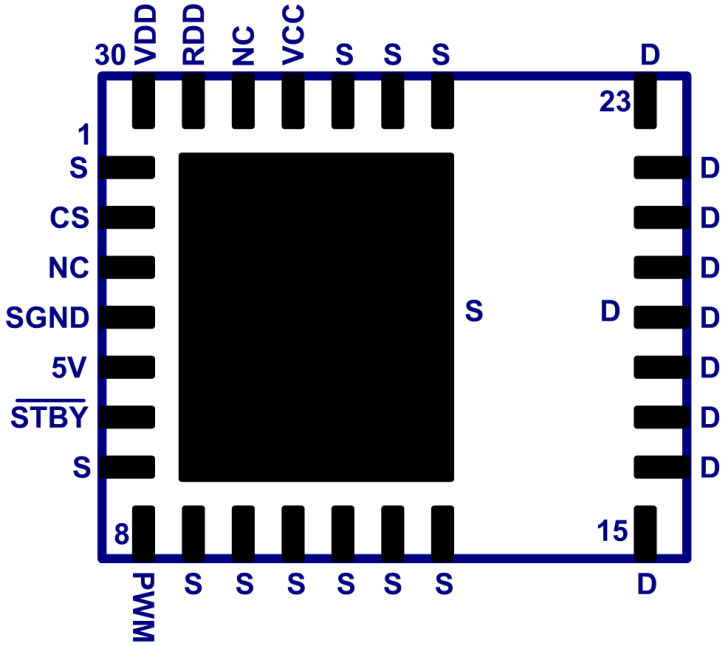


Fig. 19. Package Top View

Pin		I/O(1)	Description
Number	Symbol		
4	S_{GND}	I	Connect directly to Source PAD
30	V_{DD}	I	Gate drive supply voltage.
29	R_{DD}	I/O	Gate drive turn-on current set pin (using R_{DD} for dV/dt control)
2	CS	O	GaN FET I_{DS} current sensing set pin. Internal current source and external resistor sets current measurement level. External resistor reference is S_{GND}.
5	5V	I	5V internal supply voltage. Connect 10 nF capacitor between 5V pin and PAD
15 - 23	D	P	Drain of power FET
27	V_{CC}	P	IC supply voltage. Provided externally.
8	PWM	I	PWM input (wrt S_{GND}).
6	$\overline{\text{STBY}}$	I	Auto-standby mode input. Connect to S_{GND} to enable auto-standby
1, 7, 9-14, 24-26, PAD	S	O, G	Source of power FET & IC supply ground. Metal pad on bottom of package.
3, 28	NC	NC	Must not connect any NC pins to Source

(1) I = Input, O = Output, P = Power, G = Ground, NC = No Connect

8. Functional Description

The following functional description contains additional information regarding the IC operating modes and pin functionality.

8.1. GaN Power IC Connections and Component Values

The typical connection diagram for this GaN Power IC is shown in Fig. 20. The IC pins include drain of the GaN power FET (D), source of the GaN power FET (S), IC supply (V_{CC}), gate drive supply (V_{DD}), gate drive turn-on control SET input (R_{DD}), PWM input (PWM), separate signal GND (S_{GND}), current sensing output (CS), auto-standby mode input ($\overline{STBY}$), and 5V supply (5V). The Source pad and Source pins (S) should all be connected to the system P_{GND}. S_{GND} pin 4 must be connected directly to Source PAD underneath IC. The Source pins (S) should each be connected externally to the Source pad directly underneath the IC. The Drain Pins (D) should all be shorted together by copper in the layout (see Section 9). The external components around the IC include V_{CC} filter capacitor (C_{VCC}) connected between V_{CC} pin and S_{GND} pin, V_{DD} filter capacitor (C_{VDD}) connected between V_{DD} pin and S_{GND} pin, turn-on dV/dt set resistor (R_{DD}) connected in between V_{DD} pin and R_{DD} pin, a current sense amplitude set resistor (R_{SET}) connected between CS pin and S_{GND}, and auto-standby mode pin ($\overline{STBY}$) connected to S_{GND}. An external capacitor (C5V, 0.01uF max) is required between pin 5V and S_{GND}. This 5V pin is for internal purposes only and must not be used for biasing external circuitry.

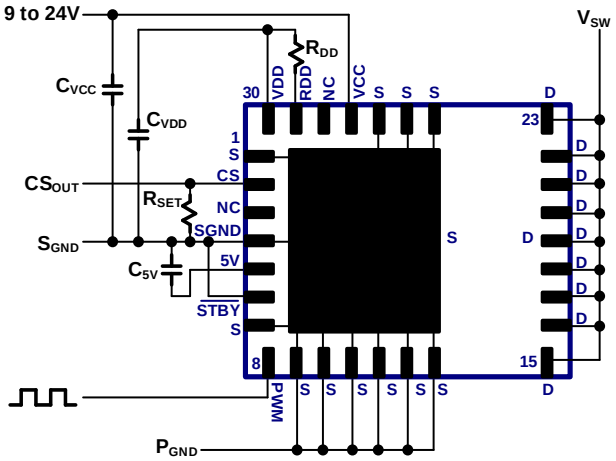


Fig. 20. IC connection diagram

The following table (Table I) shows the recommended component values (typical only) for the external components connected to the pins of this GaN power IC. These components should be placed as close as possible to the IC. Please see PCB Layout Guidelines for more information.

SYM	DESCRIPTION	TYP	UNITS
C_{VCC}	V_{CC} supply capacitor	0.1	µF
C_{VDD}	V_{DD} supply capacitor	0.010	µF
R_{DD}	Gate drive turn-on current set resistor	50	Ω
R_{SET}	Current sense amplitude set resistor	Depends on system design (See Section 8.6 , Equation 1)	Ω
C_{5V}	5V supply capacitor	10 (Max)	nF

Table I. Recommended component values (typical only).

8.2. UVLO Mode

This GaN Power IC includes under-voltage lockout (UVLO) circuits for properly disabling all of the internal circuitry when V_{CC} is below the V_{CCUV+} threshold (8.5V, typical) or V_{DD} is below the V_{DDUV+} threshold (4.5V, typical). During UVLO Mode, the internal gate drive and power FET are disabled and V_{CC} consumes a low quiescent current (275µA, typical). As the V_{CC} supply voltage increases (Fig. 21), the voltage at the V_{DD} pin also increases and exceeds V_{DDUV+}. The V_{DD} voltage continues to increase with V_{CC} until it gets limited to a constant voltage level (6.8V, typical) by the internal regulator. The V_{CC} voltage continues to increase until it exceeds V_{CCUV+} and the IC enters Normal Operating Mode. The gate drive is enabled and the control signal at the PWM input turns the internal GaN power FET on and off normally. During system power off, when V_{CC} decreases below the V_{CCUV-} threshold (7.3V, typical), the gate drive is disabled and the IC enters UVLO Mode.

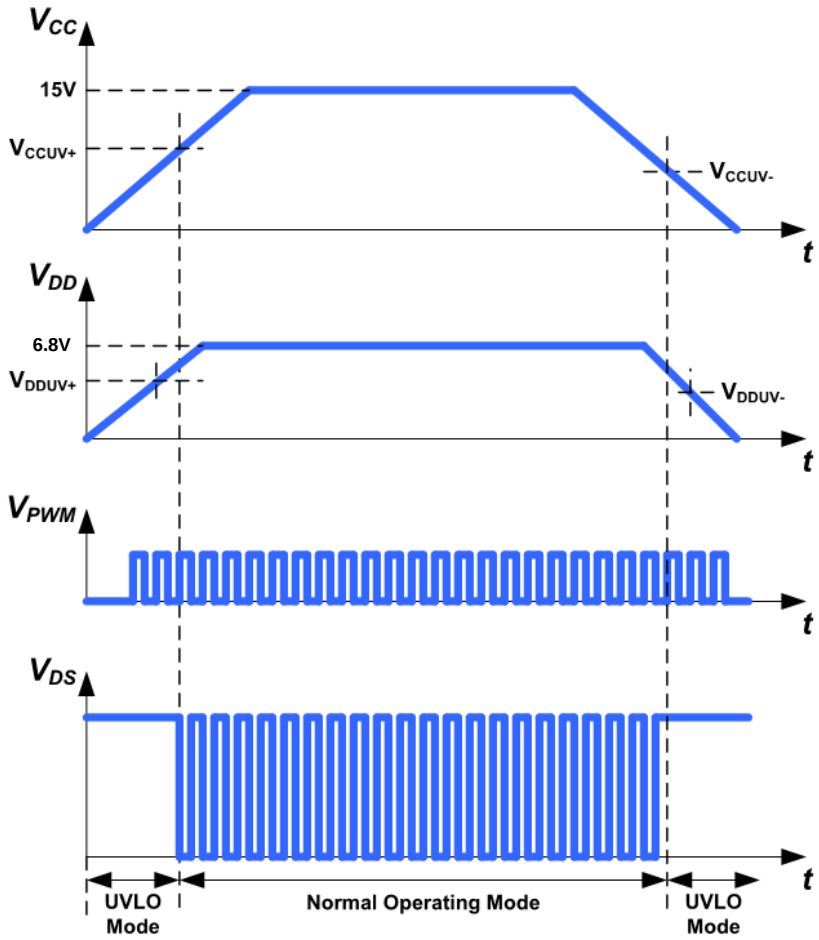


Fig. 21. UVLO Mode timing diagram

8.3. Normal Operating Mode

During Normal Operating Mode, all of the internal circuit blocks are active. V_{CC} is above 9V, V_{DD} is maintained at 6.2V by the internal voltage regulator, and the internal gate drive and power FET are both enabled. The external PWM signal at the PWM pin determines the frequency and duty-cycle of the internal gate of the power FET. As the PWM voltage toggles above and below the rising and falling input thresholds (2.8V and 1.1V), the internal power FET toggles on and off (Fig. 22). The drain of the power FET then toggles between the source voltage (power ground) and a higher voltage level (700V, max), depending on the external power conversion circuit topology. During each on-time, the CS pin outputs a voltage signal from the internal loss-less current sensing circuit. This circuit measures the current flowing in the GaN power FET without the need for an external current sensing resistor (see section 8.6 GaNSense Technology Loss-Less Current Sensing).

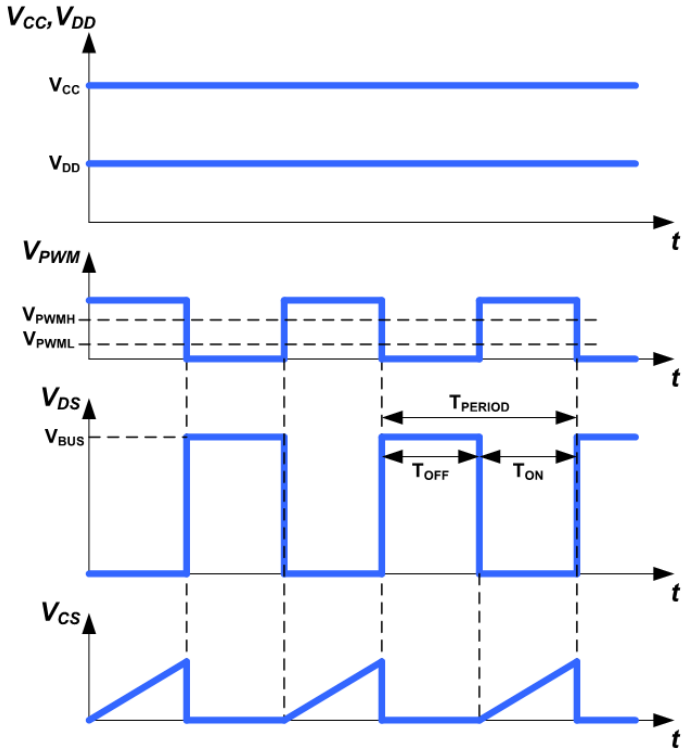


Fig. 22. Normal operating mode timing diagram

8.4. Low Power Standby Mode

This GaN Power IC includes an autonomous Low Power Standby Mode for disabling the IC and reducing the V_{CC} current consumption. During Normal Operating Mode, the PWM pin toggles high and low to turn the GaN power FET on and off. If the input pulses at the PWM pin stop and stay below the lower V_{PWML} turn-off threshold (1.1V, typical) for the duration of the internal timeout standby delay (t_{TO_STBY}, 90usec, typical), then the IC will automatically enter Low Power Standby Mode (Fig. 23). This will disable the gate drive and other internal circuitry and reduce the V_{CC} supply current to a low level (275uA, typical). When the PWM pulses restart, the IC will wake up instantly at the first rising edge of the PWM input and enter Normal Operating Mode again. To enable auto Standby Mode, the auto-standby mode pin ($\overline{STBY}$) should always be connected to S_{GND} (set low). To disable auto Standby Mode, $\overline{STBY}$ pin should be connected to the 5V pin (set high).

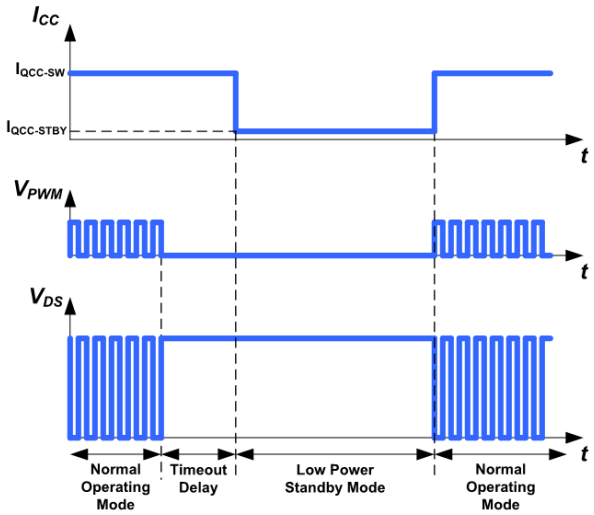


Fig. 23. Autonomous Low Power Standby Mode timing diagram

8.5. Programmable Turn-on dV/dt Control

During first start-up pulses or during hard-switching conditions, it is desirable to limit the slew rate (dV/dt) of the drain of the power FET during turn-on. This is necessary to reduce EMI or reduce circuit switching noise. To program the turn-on dV/dt rate of the internal power FET, a resistor (R_{DD}) is placed in between the V_{DD} pin 30 and the R_{DD} pin 29. This resistor (R_{DD}) sets the turn-on current of the internal gate driver and therefore sets the turn-on falling edge dV/dt rate of the drain of the power FET (Fig. 24).

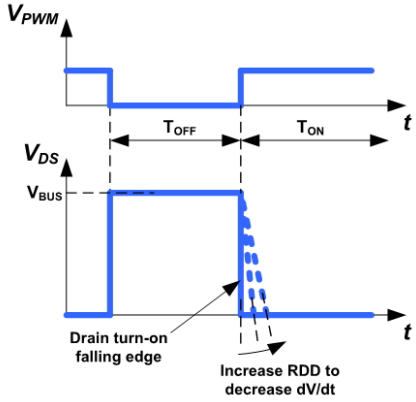


Fig. 24. Turn-on dV/dt slew rate control

Programmable Turn-on dV/dt Control (Cont.)

The NV6138C has been configured for wider RDD resistor value range. This allows for super slow turn-on dV/dt control of the GaN Power FET to reduce EMI in certain applications. The table below (Table II) shows RDD range comparison for NV6138A and NV6138C versions.

GaN IC Revision	SYM	DESCRIPTION	Min	Max	Unit
NV6138A	RDD	Gate drive turn-on set resistor	0	500	Ω
NV6138C	RDD	Gate drive turn-on set resistor	0	1000	Ω

Table II. Recommended component values (Min and Max)

8.6. GaNSense™ Technology Loss-Less Current Sensing

For many applications it is necessary to sense the cycle-by-cycle current flowing through the power FET. Existing current sensing solutions include placing a current sensing resistor in between the source of the power FET and P_{GND}. This resistor method increases system conduction power losses, creates a hotspot on the PCB, and lowers overall system efficiency. To eliminate this external resistor and hotspot, and increase system efficiency, this IC includes GaNSense™ Technology for integrated and accurate loss-less current sensing. The current flowing through the internal GaN power FET is sensed internally and then converted to a current at the current sensing output pin (CS). An external resistor (R_{SET}) is connected from the CS pin to the S_{GND} pin and is used to set the amplitude of the CS pin voltage signal (Fig. 25). This allows for the CS pin signal to programmed to work with different controllers with different current sensing input thresholds.

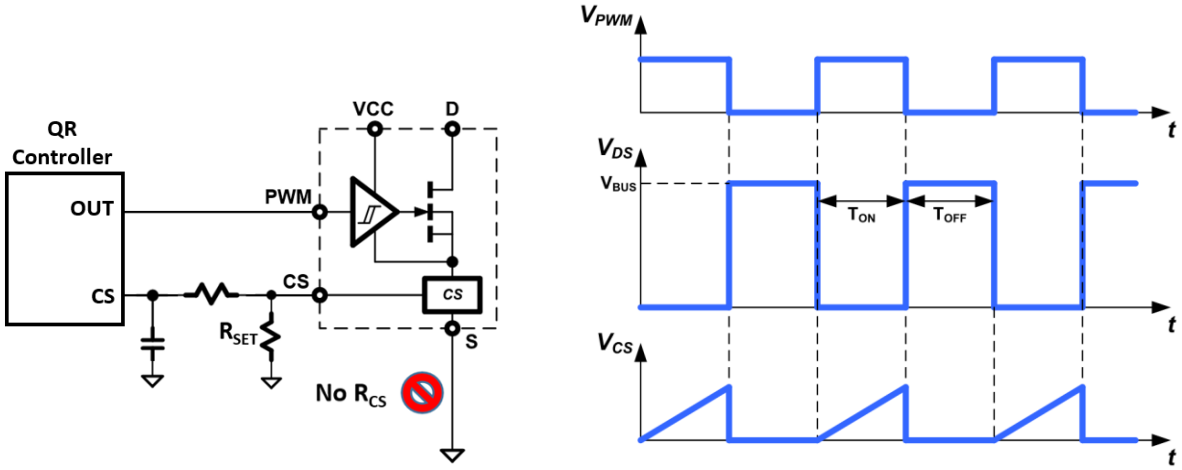


Fig. 25. Current sensing circuit and timing diagram

When comparing GaNSense™ Technology versus existing external resistor sensing method (Fig. 26), the total ON resistance, $R_{ON(TOT)}$, can be substantially reduced. For a 65W high-frequency QR flyback circuit, for example, $R_{ON(TOT)}$ is reduced from 240m to 120m. The power loss savings by eliminating the external resistor results in a +0.5% efficiency benefit for the overall system.

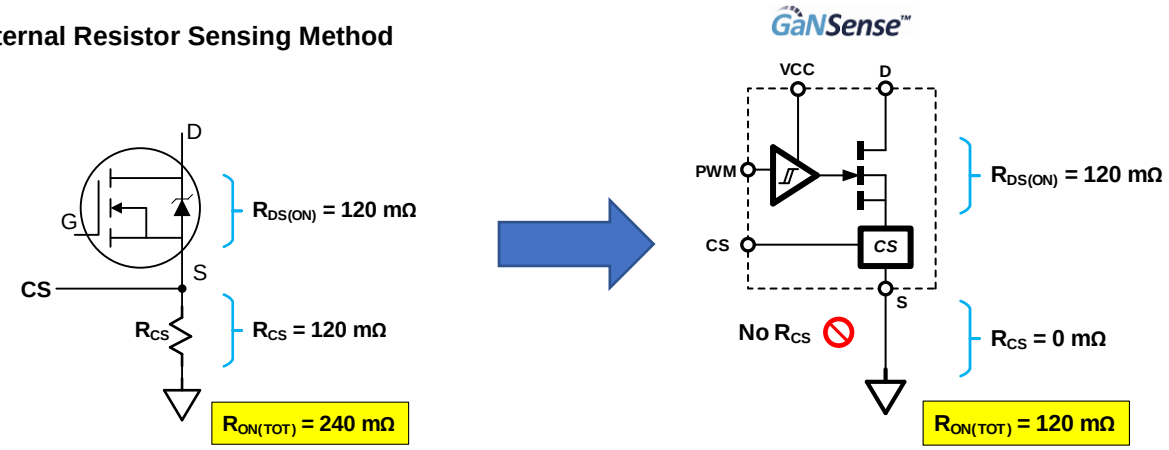


Fig. 26. External resistor sensing vs. GaNSense™ Technology

To select the correct R_{SET} resistor value, the following equation (Equation 1) can be used. This equation uses the equivalent desired external current sensing resistor value (R_{CS}), together with the gain of the internal sensing circuitry, to generate the equivalent R_{SET} resistor value. This R_{SET} value will give then give the correct voltage level at the CS pin to be compatible with the internal current sensing threshold of the system controller.

$$I_{OUT}\ Ratio = \frac{I_{DS}}{I_{CS}} = \frac{6.21A}{0.00125A} = 4968$$

$$R_{SET} = \ 4968 * R_{CS}$$

$$4968 * 120m\Omega = 596.16\Omega$$

8.7. Over Current Protection (OCP)

This GaN Power IC includes cycle-by-cycle over-current detection and protection (OCP) circuitry to protect the GaN power FET against high current levels. During the on-time of each switching cycle, should the peak current exceed the internal OCP threshold (1.9V, typical), then the internal gate drive will turn the GaN power FET off quickly and truncate the on-time period to prevent damage from occurring to the IC. The IC will then turn on again at the next PWM rising edge at the start of the next on-time period (Fig. 27). This OCP protection feature will self-protect the IC each switching cycle against fast peak over current events and greatly increase the robustness and reliability of the system. The actual peak current threshold can be calculated using Equation 2 and is a function of the internal current-sensing ratio and the external R_{SET} resistor. The internal OCP threshold (1.9V, typical) is much higher than the OCP thresholds of many popular QR, ACF and PFC controllers. This ensures good compatibility of this IC with existing controllers without OCP threshold conflicts.

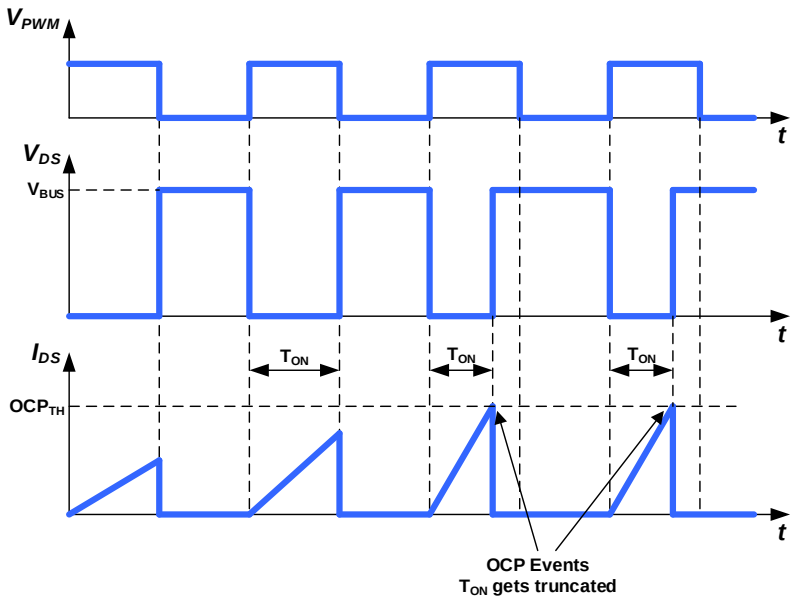


Fig. 27. OCP threshold timing diagram

$$I_{OCP} = \frac{[\ 1.9\ \text{V x}\ 4968\ ]}{R_{SET}}$$

Equation 2. OCP current threshold equation

8.8. Over Temperature Protection (OTP)

This GaN Power IC includes over-temperature detection and protection (OTP) circuitry to protect the IC against excessively high junction temperatures (T_J). High junction temperatures can occur due to overload, high ambient temperatures, and/or poor thermal management. Should T_J exceed the internal T_{OTP+} threshold (165C, typical) then the IC will latch off safely. When T_J decreases again and falls below the internal T_{OTP-} threshold (105C, typical), then the OTP latch will be reset. Until then, internal OTP latch guaranteed to remain in the correct state while V_{CC} is greater than 5V. During an OTP event, this GaN IC will latch off and the system V_{CC} supply voltage will decrease due to the loss of the aux winding supply. The system V_{CC} will fall below the lower UV- threshold of the controller and the high-voltage start-up circuit will turn-on and V_{CC} will increase again (Fig. 28). V_{CC} will increase above the rising UV+ threshold and the controller turn on again and deliver PWM pulses again.

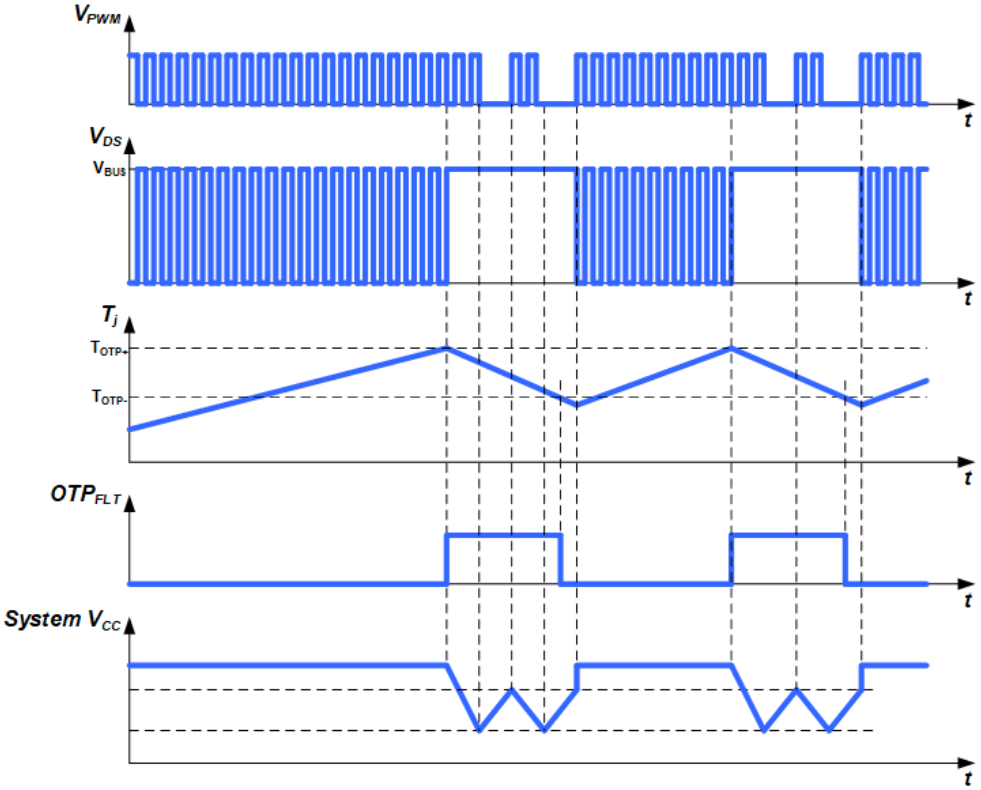


Fig. 28. OTP threshold timing diagram

8.9. Drain-to-Source Voltage Considerations

GaN Power ICs have been designed and tested to provide significant design margin to handle transient and continuous voltage conditions that are commonly seen in single-ended topologies, such as quasi-resonant (QR) flyback applications. The different voltage levels and recommended margins in a typical QR flyback can be analyzed using Fig. 29. When the device is switched off, the energy stored in the transformer leakage inductance will cause V_{DS} to overshoot to the level of V_{SPIKE}. The clamp circuit should be designed to control the magnitude of V_{SPIKE}. After dissipation of the leakage energy, the device V_{DS} will settle to the level of the bus voltage plus the reflected output voltage which is defined in Fig. 29 as V_{DS-OFF}.

- For repetitive events, 80% derating should be applied from $V_{DS\ (TRAN)}$ rating (800V) to 640V max under the worst case operating conditions.
- It is recommended to design the system such that V_{DS-OFF} is derated 80% from the $V_{DS(CONT)}$ (700V) max rating to 560V.
- For half-bridge based topologies, such as LLC, V_{DS} voltage is clamped to the bus voltage. V_{DS} should be designed such that it meets the V_{DS-OFF} derating guideline (560V).
- Non-repetitive events are infrequent, one-time conditions such as line surge, ESD, and lightning. No derating from the $V_{DS(TRAN)}$ rating (800V) is needed for non-repetitive V_{SPIKE} durations < 100 µs. The $V_{DS(TRAN)}$ rating (800V) allows for repetitive events that are <400ns, with 80% derating required (for example repetitive leakage inductance spikes).

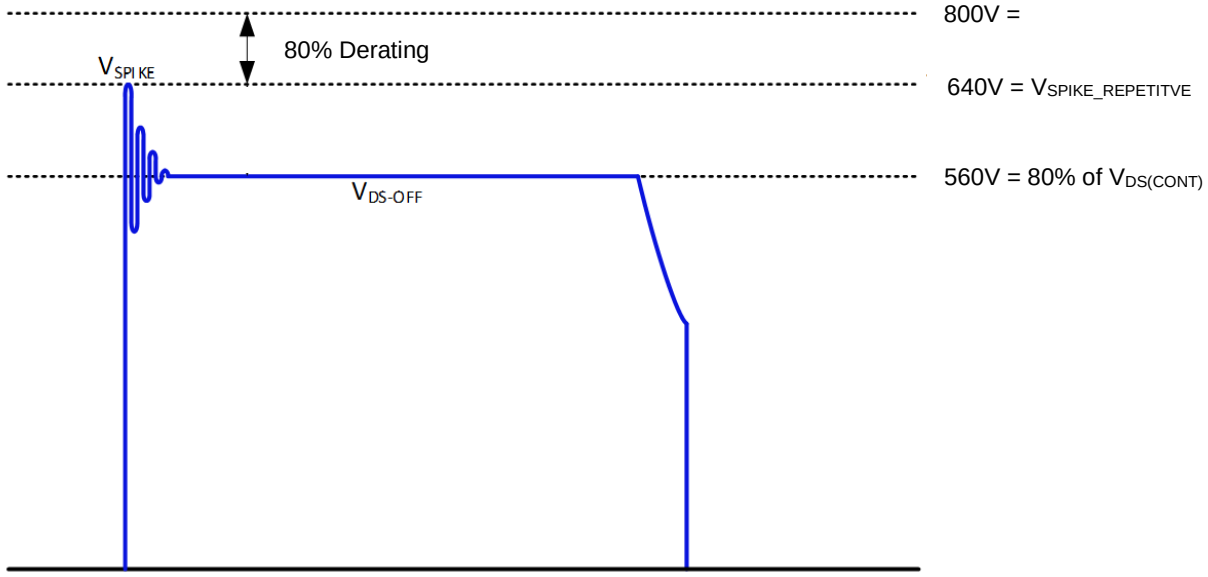
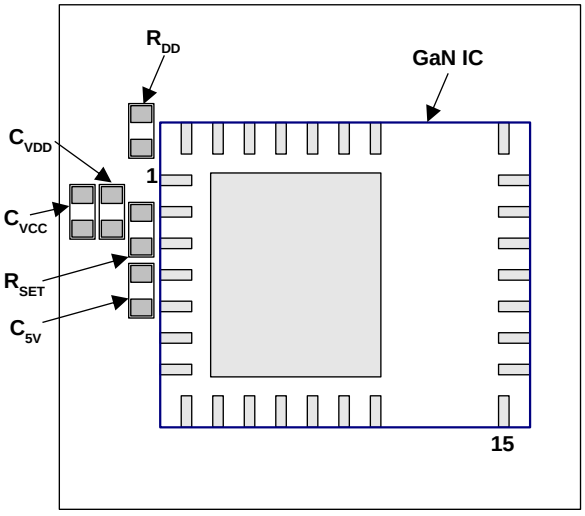


Fig. 29. QR flyback drain-to-source voltage stress diagram

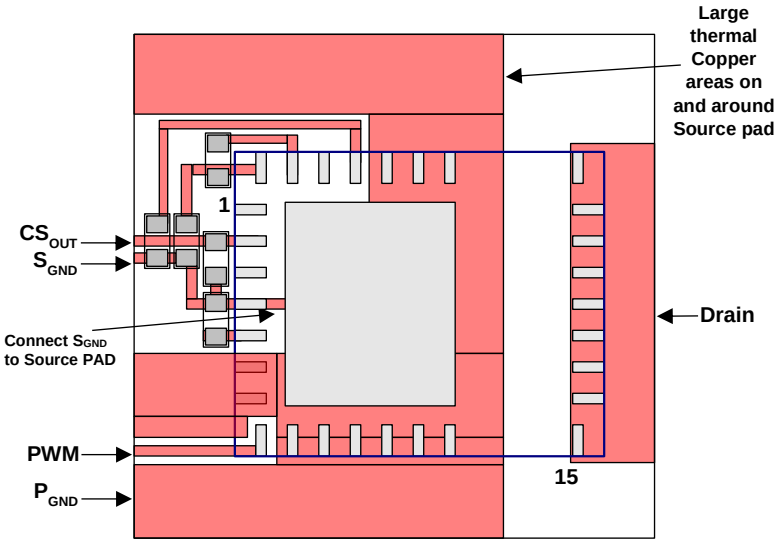
9. PCB Layout Guidelines

For best electrical and thermal results, these PCB layout guidelines (and 4 steps below) must be followed:

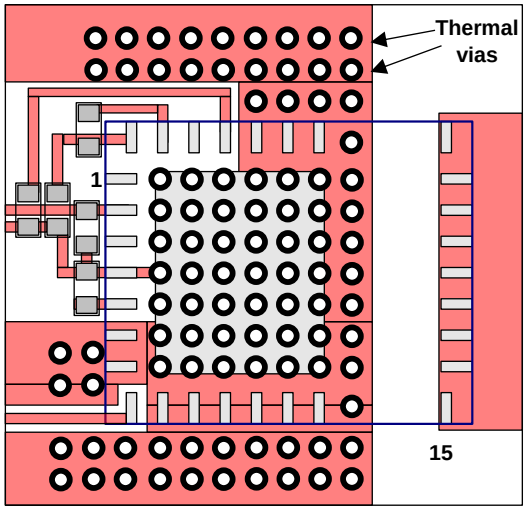
1) Place IC components as close as possible to the GaN IC. Place R_{SET} resistor directly next to CS pin to minimize high frequency switching noise.
2) Connect the ground of IC components to S_{GND} pin 4 to minimize high frequency switching noise. Connect S_{GND} pin 4 directly to Source PAD underneath IC.
3) Route all connections on single layer. This allows for large thermal copper areas on other layers.
4) Place large copper areas on and around Source pad.
5) Place many thermal vias inside Source pad and inside source copper areas.
6) Place large as possible copper areas on all other layers (bottom, top, mid1, mid2).



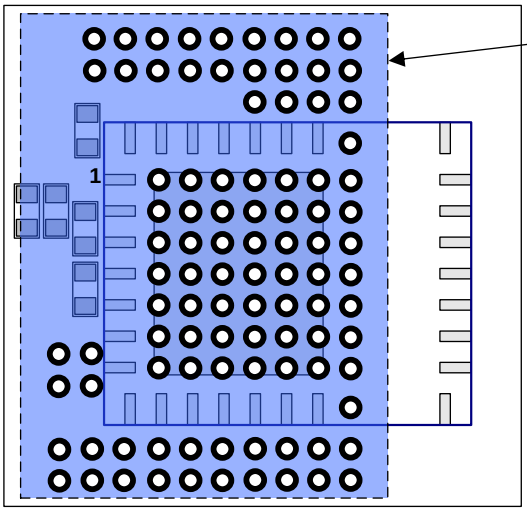
Step 1. Place GaN IC and components on PCB. Place components as close as possible to IC!



Step 2. Route all connections on single layer. Make large copper areas on and around Source pad!

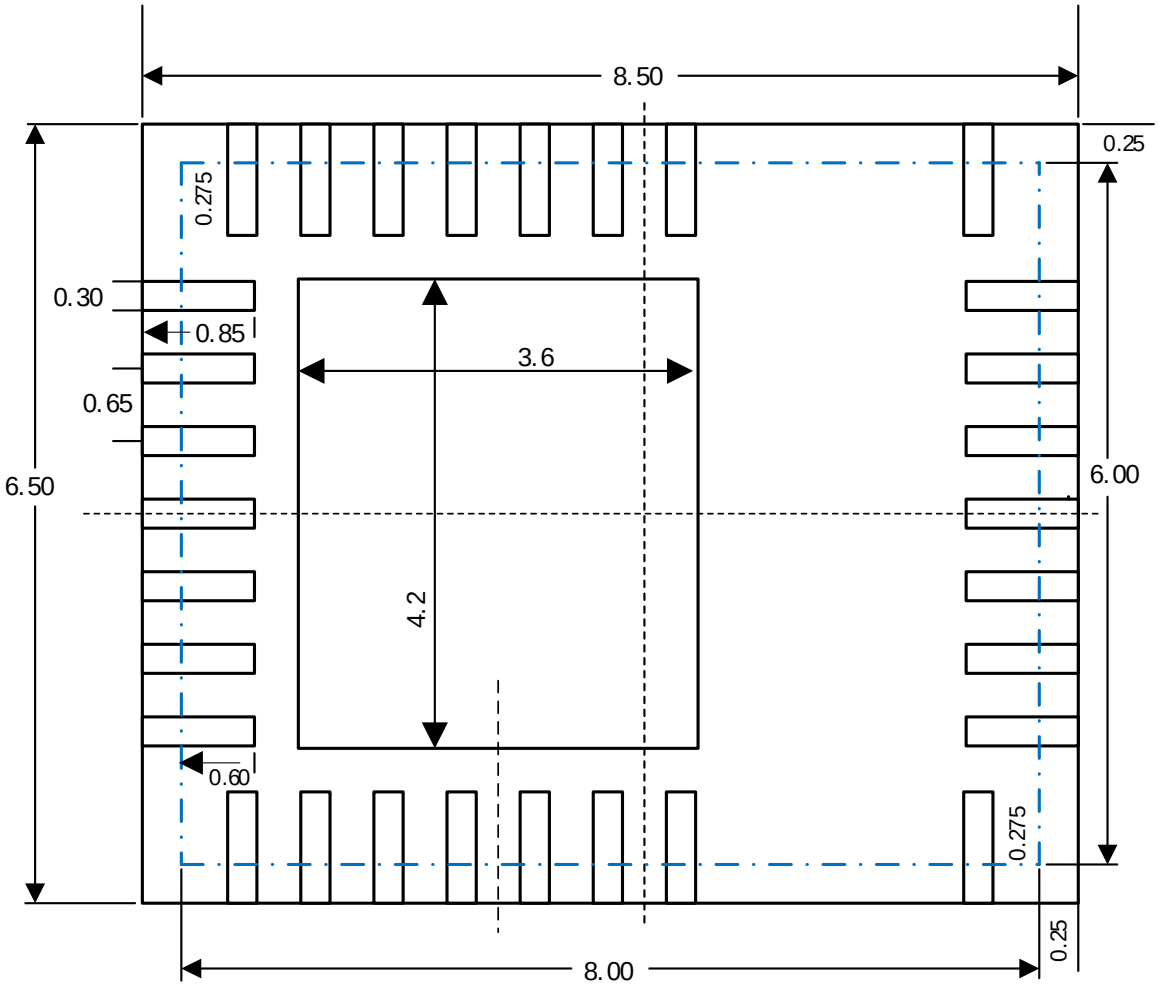


Step 3. Place many thermal vias inside source pad and inside source copper areas. (dia=0.65mm, hole=0.33mm, pitch=0.925mm, via



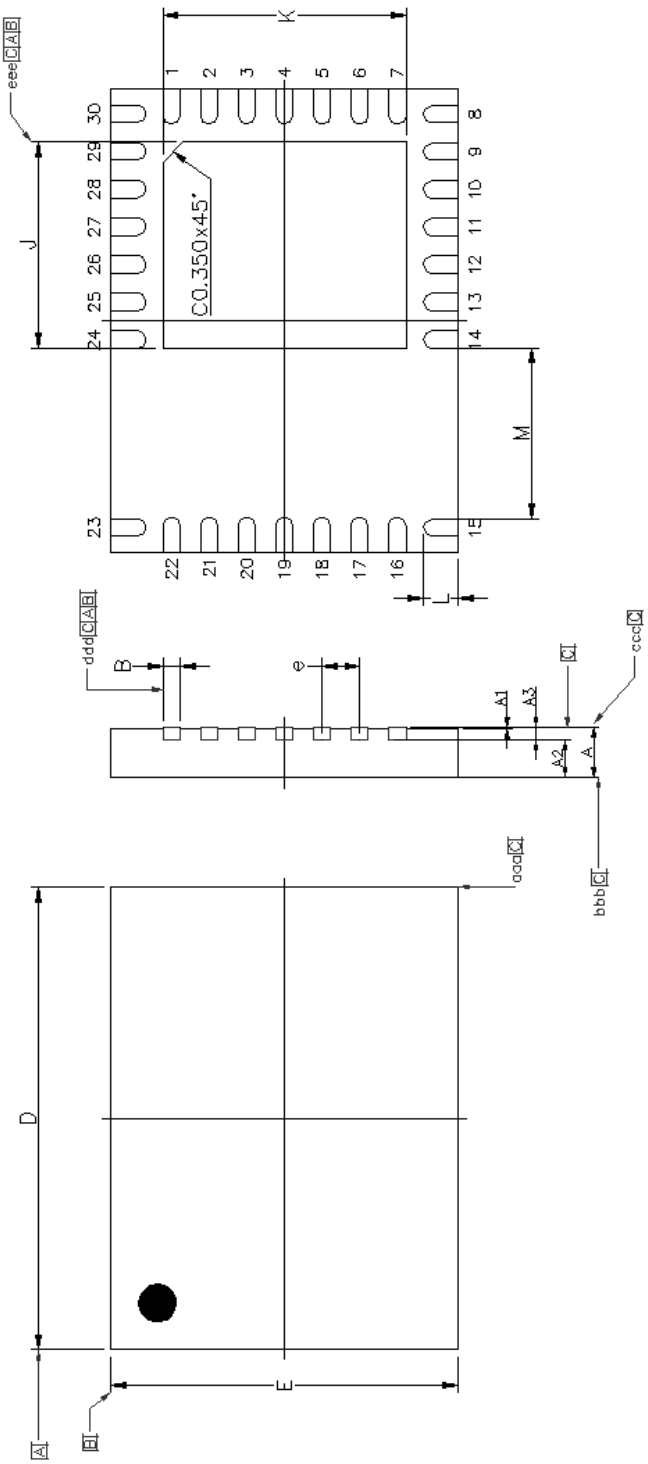
Step 4. Place large copper areas on other layers. Make all thermal copper areas as large as

10. Recommended PCB Land Pattern



All dimensions are in mm

11. Package Outline (Power QFN)

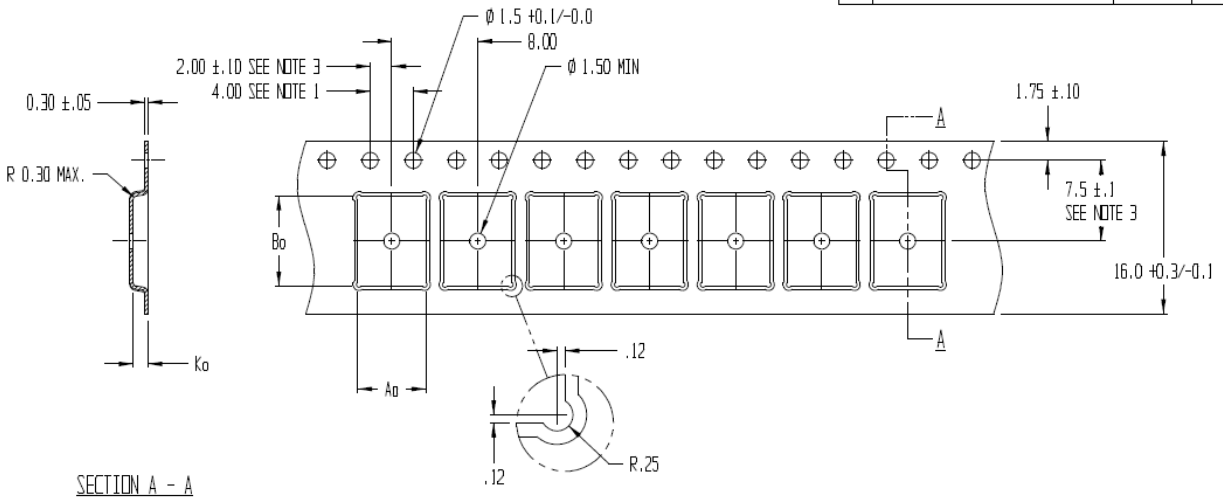


		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.8	0.85	0.9
STAND OFF		A1	0.00	0.02	0.05
MOLD THICKNESS		A2	---	0.65	---
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		B	0.25	0.3	0.35
BODY SIZE	X	D		8.00 BSC	
	Y	E		6.00 BSC	
LEAD PITCH		e		0.65 BSC	

		SYMBOL	MIN	NOM	MAX
EP SIZE	X	J	3.5	3.6	3.7
	Y	K	4.1	4.2	4.3
LEAD LENGTH		L	0.55	0.6	0.65
HIGH VOLTAGE SPACING		M	2.85	2.95	3.05
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		bbb		0.1	
COPLANARITY		ccc		0.08	
LEAD OFFSET		ddd		0.1	
EXPOSED PAD OFFSET		eee		0.1	

12. Tape and Reel Dimensions

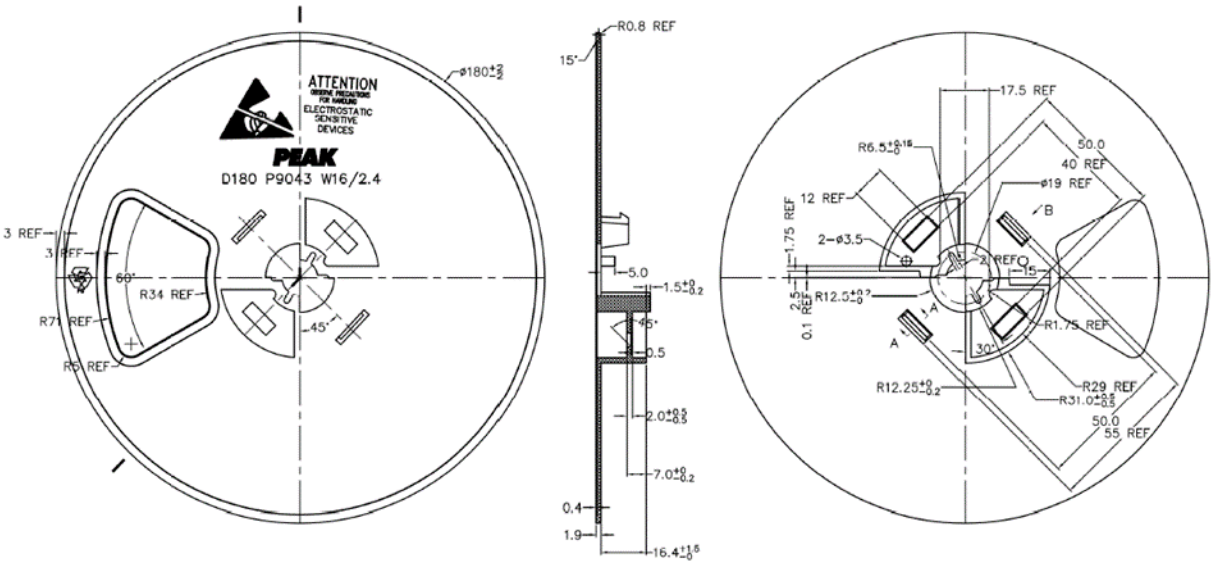
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



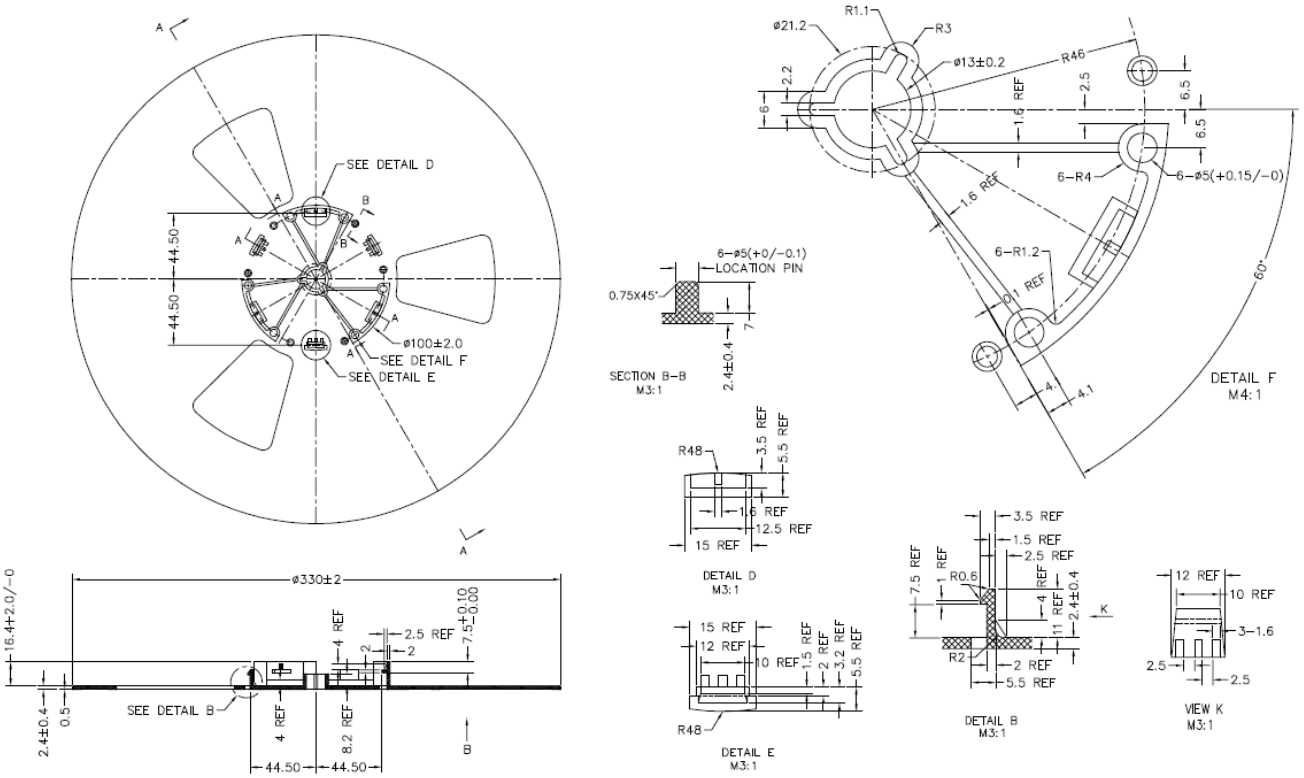
Ao = 6.35
Bo = 8.35
Ko = 1.40

12. Tape and Reel Dimensions (Cont.)

7” Reel



13” Reel



13. Ordering Information

Part Number	Operating Temperature Grade	Storage Temperature Range	Package	MSL Rating	Packing (Tape & Reel)
NV6138C-RA	-55°C to +150°C T_{CASE}	-55°C to +150°C T_{CASE}	6 x 8 mm PQFN	3	1,000: 7” Reel
NV6138C	-55°C to +150°C T_{CASE}	-55°C to +150°C T_{CASE}	6 x 8 mm PQFN	3	5,000: 13” Reel

14. 20-Year Limited Product Warranty

The 20-year limited warranty applies to all packaged Navitas GaNFast Power ICs in mass production, subject to the terms and conditions of, Navitas' express limited product warranty, available at https://navitassemi.com/terms-conditions. The warranted specifications include only the MIN and MAX values only listed in Absolute Maximum Ratings, ESD Ratings and Electrical Characteristics sections of this datasheet. Typical (TYP) values or other specifications are not warranted.

15. Revision History

Date	Status	Notes
Sept. 17, 2023	PRELIMINARY	First publication
June 13, 2024	FINAL	First publication

Additional Information

Contact info@navitassemi.com