iS20M5R5S1T

SuperQ™ 200V N-Channel Power MOSFET

FEATURES

- Industry leading $R_{DS(on)}$ in TOLL package
- High short-circuit withstand capability (SCWC)
- 100% UIS tested in production
- Low switching losses, Q_{SW} and E_{OSS}
- Easier parallelling with ± 0.5V gate threshold

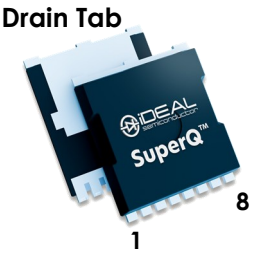
APPLICATIONS

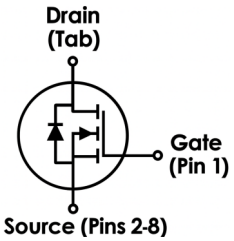
- Motor control
- Boost converters and SMPS control FETs
- Secondary side synchronous rectifier

DESCRIPTION

Engineered for high-efficiency SMPS and motor drives, this 200V SuperQ MOSFET delivers ultra-low conduction and switching losses in a robust TOLL package. Featuring best-in-class $R_{DS(on)}$ and Q_{SW}, it minimizes heat dissipation at both full and partial loads.

PRODUCT SUMMARY





TOLL

Parameter T_A = 25°C	Value	Unit
V_{DS}	200	V
$R_{DS(on),max}$	5.5	mΩ
I_D	151	A
Q_G	112	nC
Q_{SW}	8.3	nC
E_{OSS}	4.0	µJ

Pb

HAL

RoHS

ORDERING INFORMATION			
Part Number	**Package**	**Marking**	**Packaging**
iS20M5R5S1T	TOLL	iS20M5R5S1	13" 2,000pcs T&R

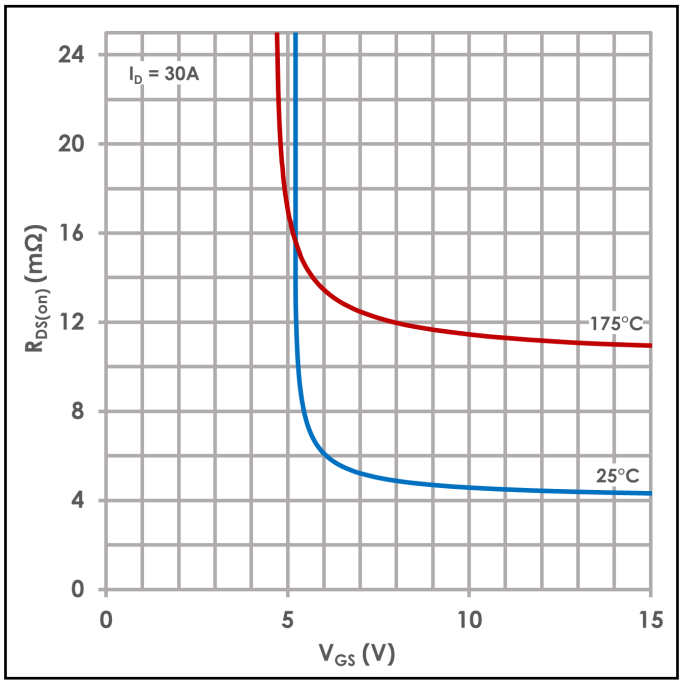


Figure 1: Typical Drain-Source On Resistance

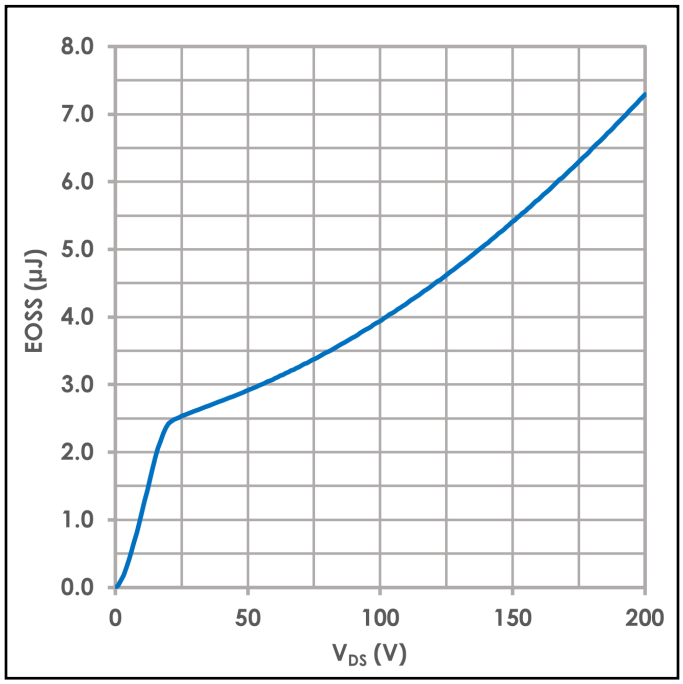


Figure 2: Typical C_{OSS} Stored Energy

ABSOLUTE MAXIMUM RATINGS			
SYMBOL	**PARAMETER** (T_A = 25°C unless otherwise specified)	**VALUE**	**UNIT**
V_{GS}	Gate-to-source voltage	± 20	V
I_D	Continuous drain current (silicon limited), T_C = 25°C	151	A
	Continuous drain current (silicon limited), T_C = 100°C	107	
I_{DM}	Pulsed drain current	538	A
P_D	Power dissipation, T_C = 25°C	314	W
T_J, T_{stg}	Operating junction, storage temperature	-55 to 175	°C
E_{AS}	Avalanche energy, single pulse I_D = 94A, R_{GS} = 25Ω	443	mJ

THERMAL CHARACTERISTICS					
SYMBOL	**PARAMETER** (T_A = 25°C unless otherwise specified)	**VALUE**			**UNIT**
		MIN	**TYP**	**MAX**	
$R_{\theta JC}$	Junction-to-case thermal resistance - TOLL	-	-	0.5	°C/W
$R_{\theta JA}$	Junction-to-ambient thermal resistance (1)	-	-	50	°C/W

(1) 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified)						
SYMBOL	PARAMETER	TEST CONDITIONS	VALUE			UNIT
			MIN	TYP	MAX	
STATIC CHARACTERISTICS						
BV_{DSS}	Drain-to-source voltage	V_{GS} = 0V, I_D = 1mA	200	-	-	V
I_{DSS}	Drain-to-source leakage current	V_{GS} = 0V, V_{DS} = 160V, T_J = 25°C	-	0.1	1	µA
		V_{GS} = 0V, V_{DS} = 160V, T_J = 125°C (2)	-	-	100	
I_{GSS}	Gate-to-source leakage current	V_{DS} = 0V, V_{GS} = 20V	-	1	100	nA
$V_{GS(th)}$	Gate-to-source threshold voltage	V_{DS} = V_{GS}, I_D = 300µA	3.1	3.5	4.1	V
$R_{DS(on)}$	Drain-to-source on-resistance	V_{GS} = 10V, I_D = 30A	-	4.6	5.5	mΩ
g_{fs}	Transconductance	V_{DS} = 10V, I_D = 30A	48	96	-	S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input capacitance (2)	V_{GS} = 0V, V_{DS} = 100V, f = 100kHz	-	8,366	10,876	pF
C_{rss}	Reverse transfer capacitance (2)		-	37	48	
C_{oss}	Output capacitance (2)		-	249	324	
$C_{o(er)}$	Effective output capacitance	V_{DS} = 0 to 100V, V_{GS} = 0V	-	396	-	
R_G	Series gate resistance	f = 1MHz	-	0.6	0.9	Ω
$t_{d(on)}$	Turn-on delay time	V_{DS} = 100V, V_{GS} = 10V, I_{DS} = 30A, $R_{G,EXT}$ = 0 Ω	-	21.5	-	ns
t_r	Rise time		-	6.6	-	
$t_{d(off)}$	Turn-off delay time		-	46.7	-	
t_f	Fall time		-	5.1	-	
GATE CHARGE CHARACTERISTICS						
Q_g	Gate charge total (2)	V_{DS} = 100V, I_D = 30A, V_{GS} = 0 to 10V	-	112	146	nC
Q_{sw}	Switching charge (3)		-	8.3	-	
Q_{gd}	Gate to drain charge (2) (3)		-	4.0	5.2	
$Q_{g(th)}$	Gate charge at threshold (3)		-	25.5	-	
Q_{gs2}	Gate to source charge (3)		-	4.3	-	
$V_{plateau}$	Gate plateau voltage		-	5.5	-	V
Q_{oss}	Output charge (2)	V_{DS} = 0 to 100V, V_{GS} = 0V	-	398	458	nC
E_{oss}	Capacitive stored energy		-	4.0	-	µJ
DIODE CHARACTERISTICS						
V_{SD}	Diode forward voltage	I_{SD} = 30A, V_{GS} = 0V	-	0.9	1.2	V
Q_{rr}	Reverse recovery charge	V_{DS} = 100V, I_F = 30A, di/dt = 100A/µs	-	0.7	-	µC
t_{rr}	Reverse recovery time		-	151	-	ns

(2) Defined by design. Not subject to production test.

(3) Q_{SW} should be used for switching loss calculations. See Figure 16 for gate charge definitions. For more information see Qsw application note on www.idealsemi.com

Ratings and Characteristics Curves

(T_A = 25°C unless otherwise specified)

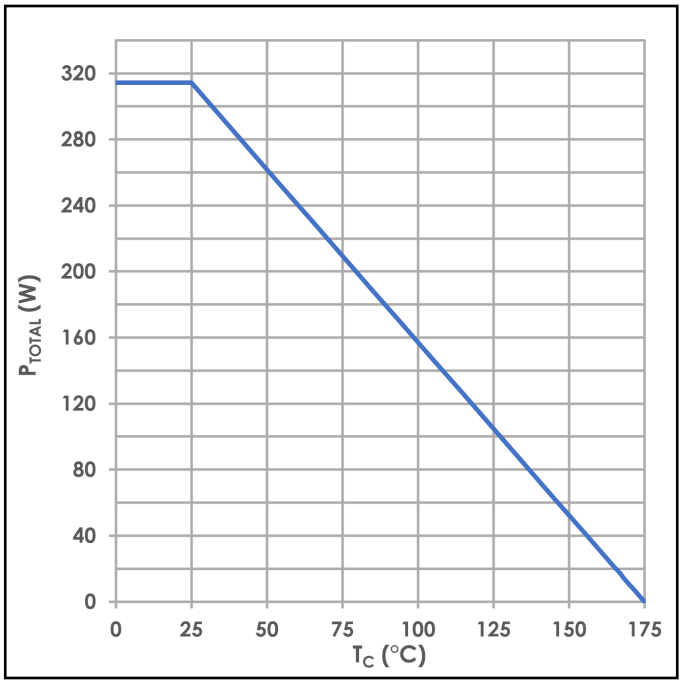


Figure 3: Power Dissipation

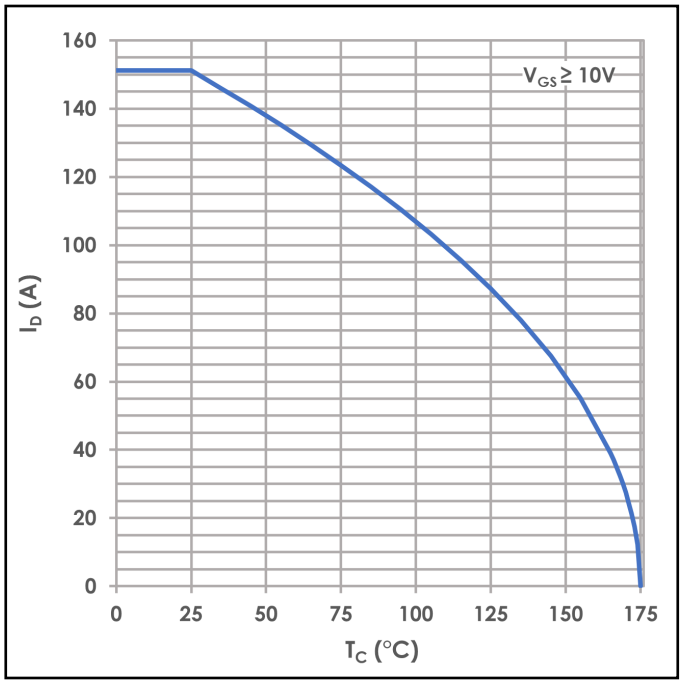


Figure 4: Drain Current

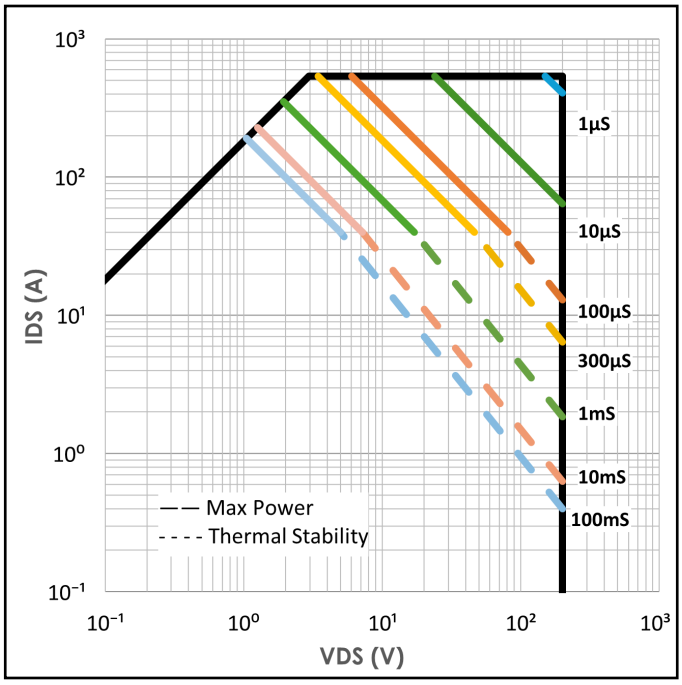


Figure 5: Safe Operating Area

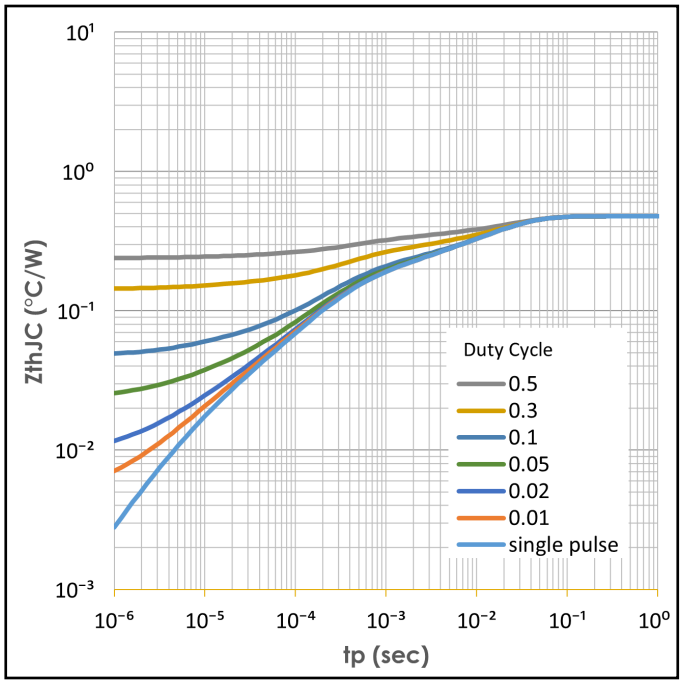


Figure 6: Max Transient Thermal Impedance

Ratings and Characteristics Curves

(T_A = 25°C unless otherwise specified)

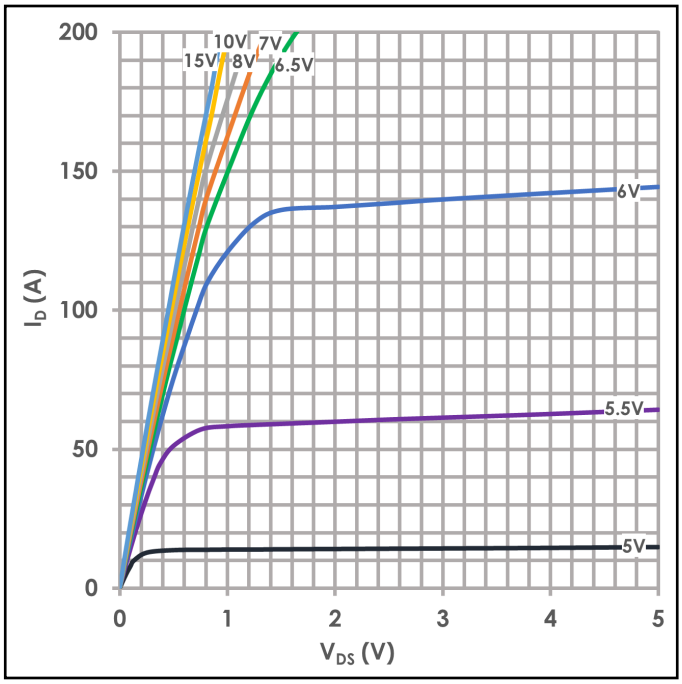


Figure 7: Typical Output Characteristics

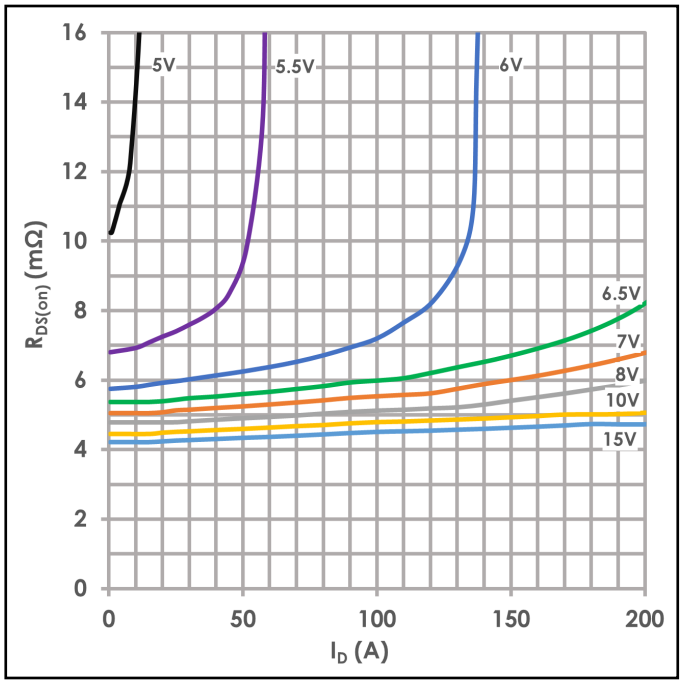


Figure 8: Typical Drain-Source On-Resistance

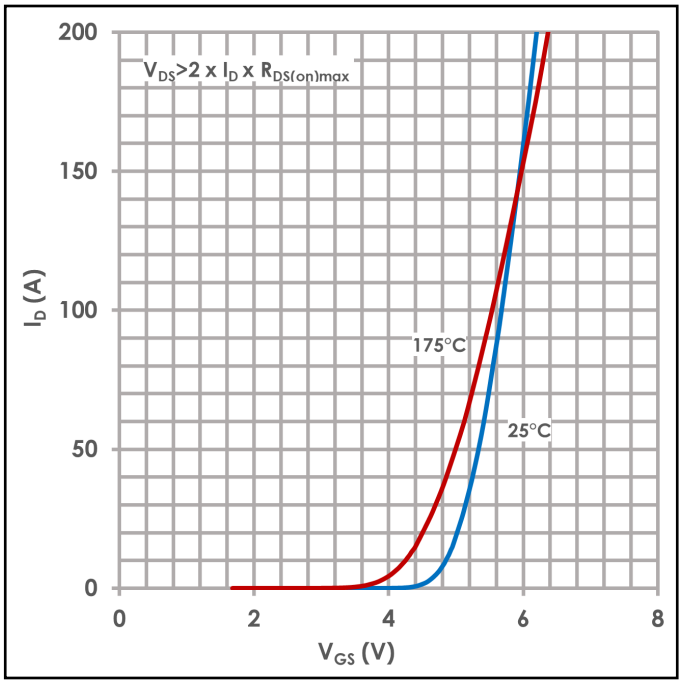


Figure 9: Typical Transfer Characteristics

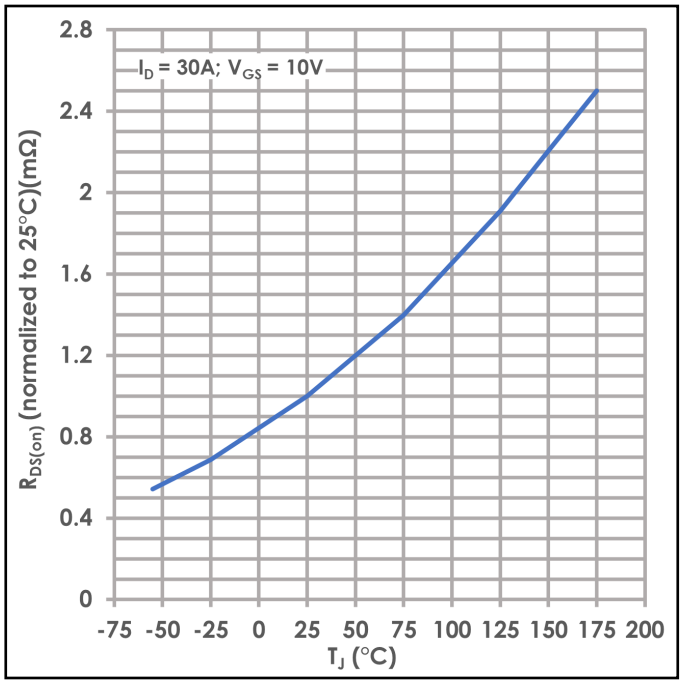


Figure 10: Normalized On-State Resistance vs. Temperature

Ratings and Characteristics Curves

(T_A = 25°C unless otherwise specified)

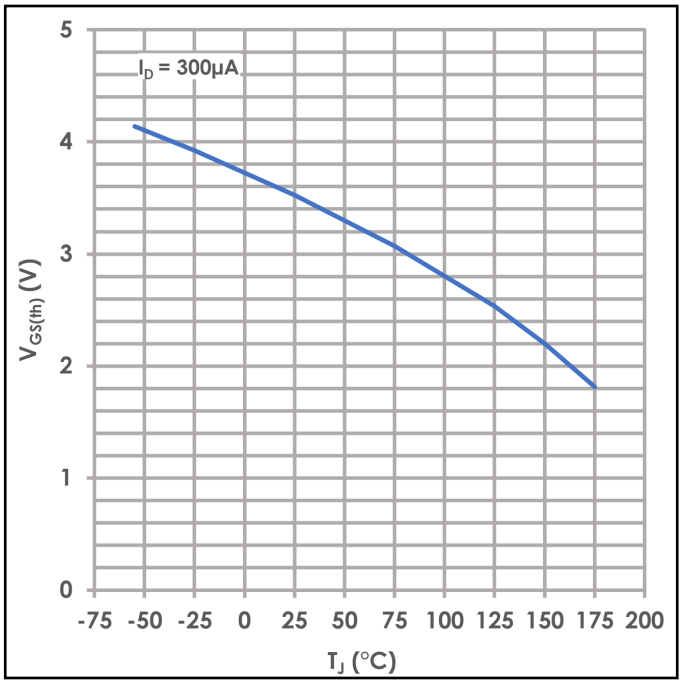


Figure 11: Typical Threshold Voltage

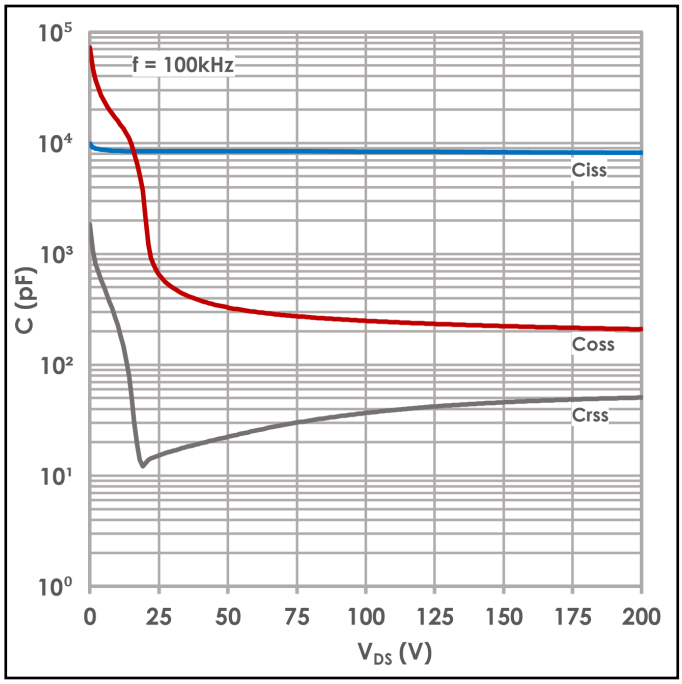


Figure 12: Typical Capacitances

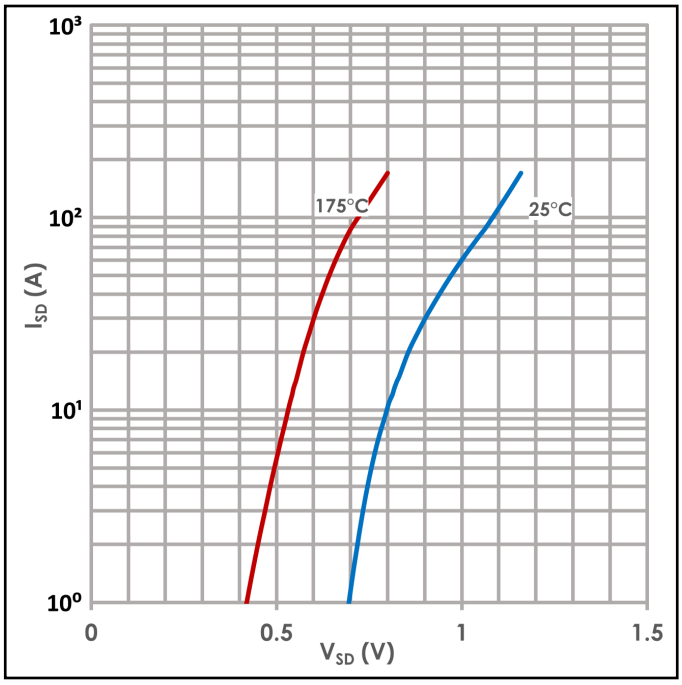


Figure 13: Typical Diode Forward Volltage

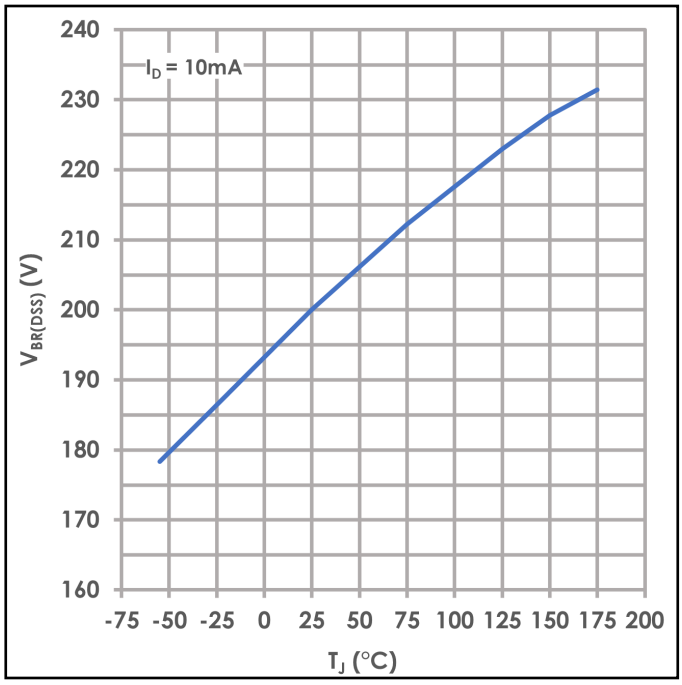


Figure 14: Min Drain-Source Breakdown Voltage

Ratings and Characteristics Curves

(T_A = 25°C unless otherwise specified)

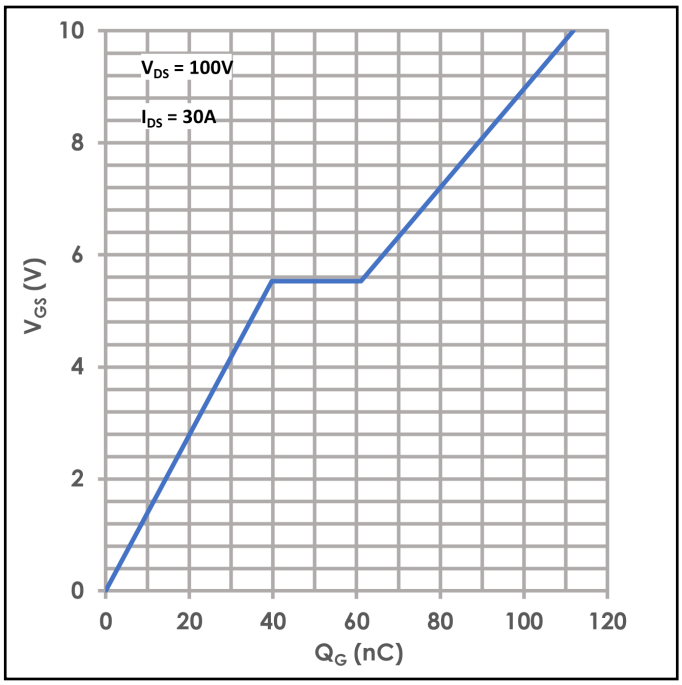


Figure 15: Typical Gate Charge

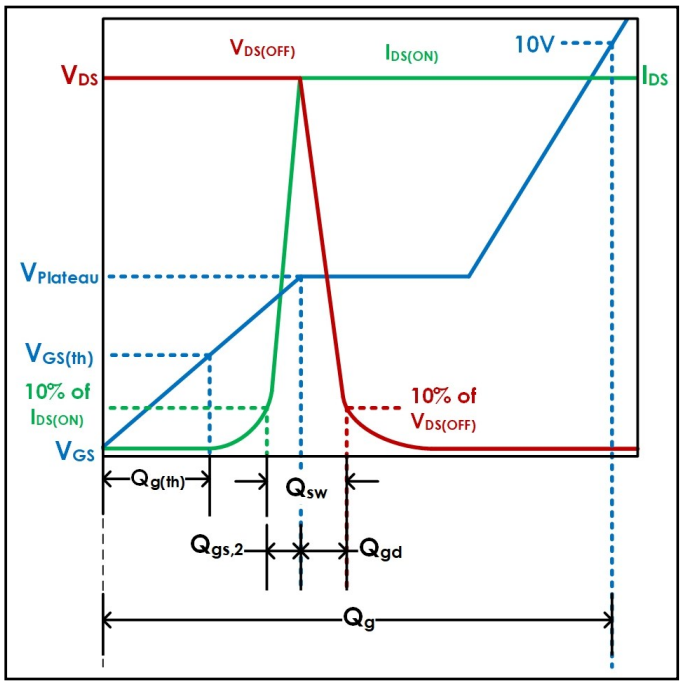
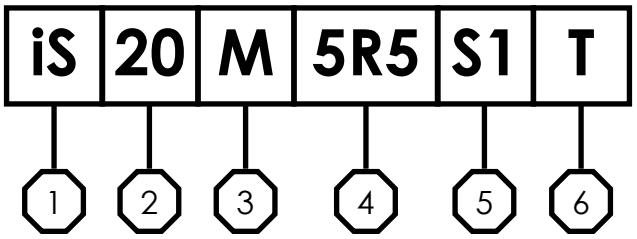


Figure 16: Gate Charge Definitions

DEVICE DECODER RING

Device Code



1 – iDEAL Semiconductor product

2 – Voltage rating divided by 10 (200V)

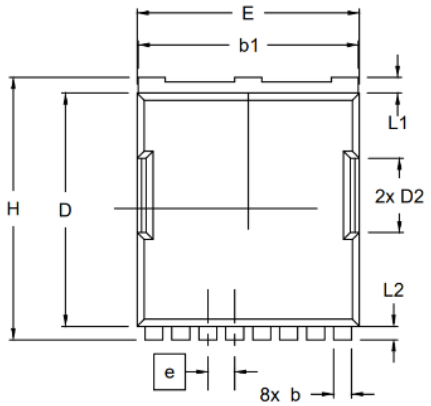
3 – M = N-Channel MOSFET, Standard Threshold

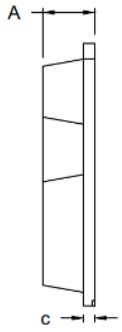
4 – Maximum drain-to-source resistance

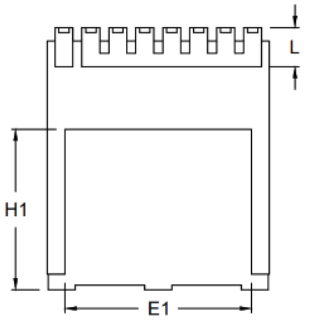
5 – SuperQ™ Generation

6 – T = TOLL

TOLL Package Drawing







SYMBOL	MIN	MAX
A	2.20	2.40
b	0.70	0.90
b1	9.70	9.90
c	0.40	0.6
D	10.28	10.58
D2	3.10	3.50
E	9.70	10.00
E1	7.90	8.60
e	1.20 BSC	
H	11.48	11.880
H1	6.75	7.43
L	1.40	2.10
L1	0.60	0.80
L2	0.500	0.700
θ	10° REF	

Notes:
1. All linear dimensions in millimeters

Revision History		
Version	**Date**	**Comments**
1.0	January 2026	Initial Release
1.1	February 2026	Modified EAS in Abs Max, GFS, Qgs2, td(on), tr, td (off), tf, Fig 12. Typ Capacitances (scale), Changed order of plots and plot numbers

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